OPERATION OF INVERSE MODE SIGE HBTS AND ULTRA-SCALED CMOS DEVICES IN EXTREME ENVIRONMENTS

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OPERATION OF INVERSE MODE SIGE HBTS AND ULTRA-SCALED CMOS DEVICES IN EXTREME ENVIRONMENTS

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To my family and friends

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SUMMARY

The objective of this work is to investigate the performance of SiGe HBTs and scaled CMOS devices in extreme environments. In this work, the inverse mode operation of SiGe HBTs is investigated as a potential solution to the vulnerability of SiGe HBTs to single event effects. The performance limitations of SiGe HBTs operating in inverse mode are investigated through an examination of the effects of scaling on inverse mode performance and optimization schemes for inverse mode performance enhancements are discussed and demonstrated. In addition the performance of scaled MOSFETs, that constitute the digital backbone of any BiCMOS technology, is investigated under radiation exposure and cryogenic temperatures. The results of this work have been published in [37, 45, 46, 47, 48, 58, 59].

Extreme environments and their effects on semiconductor devices are introduced in Chapter 1. The immunity of 90nm MOSFETs to total ionizing dose damage under proton radiation is demonstrated.

Inverse mode operation of SiGe HBTs is introduced in Chapter 2 as a potential radiation hard solution by design. The effect of scaling on inverse mode performance of SiGe HBTs is investigated and the performance limitations in inverse mode are identified.

Optimization schemes for improving inverse mode performance of SiGe HBTs are discussed in Chapter 3. Inverse mode performance enhancement is demonstrated experimentally in optimized device structures manufactured in a commercial third generation SiGe HBT BiCMOS platform. Further, a cascode device structure, the combines the radiation immunity of an inverse mode structure with the performance of a forward mode common emitter device is

discussed. Finally, idealized doping profiles for inverse mode performance enhancement is discussed through TCAD simulations.

The cryogenic performance of inverse mode SiGe HBTs are discussed in Chapter 4. A novel base current behavior at cryogenic temperature is identified and its effect on the inverse mode performance is discussed.

Matching performance of a 90nm bulk CMOS technology at cryogenic temperatures is investigated experimentally and through TCAD simulations in Chapter 5. The effect of various process parameters on the temperature sensitivity of threshold voltage mismatch is discussed. The potential increase of mismatch in subthreshold MOSFETs operating in cryogenic temperatures due to hot carrier effects is also investigated.

Chapter 1

Introduction and Motivation

This chapter provides a brief overview of the challenges and opportunities of extreme environment electronics and demonstrates how off-the-shelf Silicon-Germanium heterojunction bipolar transistor (SiGe HBT) technology and scaled CMOS devices could potentially offer equally reliable but significantly cheaper alternatives to radiation hardened devices for extreme environment applications.

The first section in the chapter introduces the extreme environments of interest in the examined work. SiGe HBT technology is introduced in the second section and its unique capabilities with respect to extreme environments is discussed in the following section. A 90 nm strained silicon CMOS technology is then introduced as a promising candidate for extreme environment applications and its hardness to ionizing dose is demonstrated. Some of the results discussed in this chapter have been published earlier in [45].

1.1 Extreme Environments

Extreme environment (EE) electronics refers to electronic devices/circuits that operate in conditions that fall outside the realm of commercial and military specifications. EE applications constitute a niche but technologically important and lucrative market for electronics. Some of the important applications that fall under EE's include deep space explorations, satellite missions (both medium and low earth orbits), cryogenically cooled detectors, oil exploration, aerospace

systems and automobiles [1]. Operating electronics in EE could involve exposing them to low, high and variable temperature and pressure, high energy radiation particles, vibration, and corrosive chemicals. While each of the above conditions poses challenges for reliable electronic circuitry, our discussion will focus exclusively on the effects of temperature and radiation on electronic devices; in particular we will be focusing on the operation of SiGe HBTs and MOSFETs in extreme environments.

Variable temperature exponentially alters the response of semiconductor devices and constitutes the most challenging aspect of device design for extreme environments. The temperature sensitivity of semiconductor devices restricts their use to a limited range of temperatures. For commercial applications, semiconductor components are typically rated to be operable from 0ºC to 85ºC while military applications require components to have an extended range of operable temperatures from -55ºC to +125ºC. EE applications require components to be operable beyond even the extended military range of temperatures. For example, deep space applications require electronic systems to be operable at temperatures as low as 4.2 K while some automotive and aerospace applications require circuits that are operable at 300ºC. Further, applications like a mission to the moon would involve extreme temperature cycling, with temperatures varying from as high as +120ºC to as low as -230ºC in a single day.

The second major challenge of operating in EE's arises due to the exposure of electronic components to high and low energy radiation particles typically encountered in space missions. Interaction of high energy particles with electronic components degrades their performance and causes additional leakage. The damaging effects of radiation can broadly be classified into three

categories [2]: 1. Total ionizing dose effects (TID) 2. Displacement damage and 3. Single event effects.

Total ionizing dose effects refer to the ionizing damage caused by the interaction of energetic charge particles with semiconductor isolation/insulation oxides. Charged particles, when traveling through the oxides, transfer some of their energy to the oxide leading to the creation of electron-hole pairs. While the electrons typically diffuse out of the oxide due to their higher diffusivity, holes get trapped and progressively create a net positive charge in the oxide. Further, some of the holes diffuse to the interface between the oxide and silicon, leading to the creation of interface traps. In bipolar transistors, this typically leads to increased recombination resulting in higher base current and lower current gain. In MOSFETs, the creation of fixed and interface traps in the gate oxide, changes the threshold voltage and leads to a decrease in transconductance and drive currents. At high enough dose, the traps in the oxide create a direct leakage path from the gate to the body/source/drain rendering the device unusable. In addition, charge accumulation in the shallow trench isolation oxides (STI), due to TID damage, create a parallel current path and contribute to a significant increase in leakage current [3].

Displacement damage is usually associated with the interaction of heavier charge particles with the semiconductor lattice. The incident heavy ions displace dopant atoms from their lattice sites leading to a net reduction in the doping of semiconductor device layers, often leading to drastic changes in electrical characteristics. In addition, displacement damage is associated with a reduction in mobility and carrier lifetime which contribute to degraded device behavior [2].

Single event effects are a family of effects usually associated with the interaction of a very high energy particle with the semiconductor lattice. As a high energy particle travels through the semiconductor lattice, it transfers energy onto the lattice creating an electron-hole pair tail along its path. The created EHPs get separated by the applied electric fields in the semiconductor device and cause transient current and voltage changes in the terminals of the device. Some of the effects of these transient waveforms, like the single event gate rupture and single event burnout are destructive while the others like single event transient, single event upset and single event latchup are usually not destructive. The single event transient and upset, however cause bit errors in digital circuits and are a source of major concern for electronics in space applications [4].

Classically, unhardened bulk silicon technology was inadequate for EE applications [5]. Cryogenic temperature significantly degrades the performance of silicon bipolar transistors while exposure to high energy radiation causes unacceptable levels of damage in both bipolar and MOSFET devices. We demonstrate here, however, that modern SiGe HBTs and MOSFETs, which together constitute SiGe BiCMOS technology, are significantly more resistant to the damaging effect of high energy radiation and also show improved performance at cryogenic temperatures. This opens up the possibility of using off-the-shelf, unhardened SiGe BiCMOS technology in extreme environments. The use of off-the-shelf technology will reduce the cost of extreme environment electronics dramatically. Also, for space applications, by not enclosing electronics in a controlled ambient (the current solution), the weight of the payload as well as its reliability can be greatly improved.

1.2 SiGe HBT Technology

SiGe HBTs were the first successful bandgap engineered devices in silicon. By introducing germanium into the base of a silicon bipolar transistor, a wider bandgap emitter is realized in silicon technology. This combination of the design flexibility of bandgap engineering similar to the III-V transistors, with the manufacturability of silicon technology has made SiGe HBT technology a widely accepted solution for many analog and RF applications.

The design of a silicon BJT suffers from multiple device design and processing limitations. At a device level, the current gain and base resistance of a BJT are strongly coupled through the base doping profile. It is impossible, therefore, in a silicon bipolar transistor, to simultaneously achieve high current gain (which requires lower base doping) and low noise, high early voltage (V_A), and high maximum frequency of oscillation (f_{max}) (which require high base doping) through base doping profile design alone. Further, the reduction in bandgap due to heavy doping in the emitter reduces the efficacy of emitter engineering in increasing the current gain of the BJT.

In addition to the limitation posed by fundamental device physics, processing limitations impose a performance limitation on conventional implanted base bipolar junction transistor. In particular, it is highly challenging to achieve a narrow and well designed base with minimum junction leakage using conventional ion implantation techniques. This is because, for minimum base transit time, the peak of the boron distribution in the base has to be placed at the emitter-base junction which, however, increases the emitter-base reverse junction tunneling [6]. Also, channeling due to ion implantation limits the base width to about 100 nm.

Both the device and processing limitations of a silicon BJT can, however, be overcome by using an epitaxially grown SiGe base instead of an ion implanted silicon base. The narrow bandgap SiGe base helps decouple the base profile from many of the important device metrics of the BJT. For example, the exponential increase in current gain with germanium mole fraction allows for the use of significantly higher base doping in a SiGe HBT as compared to a silicon BJT for the same current gain. In combination with a lower temperature epitaxial base process, bandgap engineering allows SiGe HBTs to achieve, simultaneously, high current gain, high f_T and f_{max}, high V_A, low noise, and low leakage while maintaining compatibility with conventional silicon processes. This combination of high performance with the integration and cost advantages of silicon technology has helped SiGe HBTs capture a significant market share from the III-V semiconductors in the high end analog and RF market.

1.3 Scaling of SiGe HBTs

SiGe HBTs are generally classified based on their peak f_T and f_{max} values into four generations of devices. The first commercial SiGe HBT technology was introduced in 1994 and its performance metrics defines the first generation of SiGe HBTs. A first generation device uses 0.35 micron lithography and achieves a peak f_T and f_{max} of 50 GHz with a open-base breakdown voltage (BV_{CEO}) of 3.3 V [7]. Second generation SiGe HBT's are typically designed for a peak f_T and f_{max} of 100 GHz with a BV_{CEO} of 2.5 V [8]. Third generation SiGe HBTs achieve a peak f_T and f_{max} of 200 GHz with a BV_{CEO} of 1.7 V [9]. Fourth generation devices are not yet widely available commercially, but are typically reported to display peak f_T and f_{max} values greater than 300GHz with a BV_{CEO} of 1.4 V [10]. The impressive improvement in performance of SiGe

HBTs from one technological generation to the next is achieved through a combination of aggressive scaling strategies and structural innovation.

The structure of a typical first generation SiGe HBT is shown in Figure 1. The device employs shallow and deep trench isolation for minimizing parasitics, an epitaxially grown highly doped sub-collector for minimal collector resistance, a selectively implanted collector (SIC) for optimizing breakdown and high injection characteristics, a low temperature epitaxially grown graded germanium SiGe base, and an in-situ doped polysilicon emitter. The extrinsic base is implanted and self-aligned to the emitter for minimizing the base link resistance. The electrical base width is approximately 65 nm.

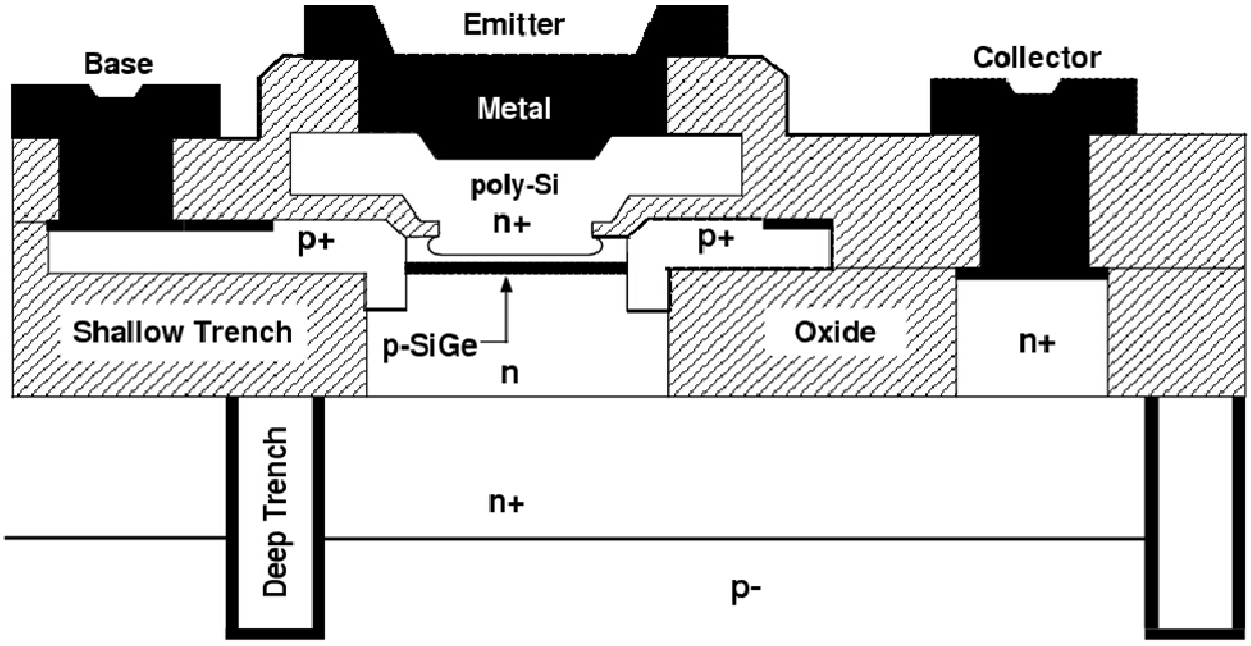


Figure 1. Structure of a typical first generation SiGe HBT

Second generation SiGe HBTs employ a similar device structure to the first generation device but achieve the improvement in performance through a mix of vertical and horizontal

scaling. An examination of the transit time equations is useful here to illustrate the scaling strategies typically employed for improving SiGe HBT performance. The total transit time (τ_{EC}) and cutoff frequency of a bipolar transistor can be expressed as [2]:

$$\tau_{EC} = \frac{kT}{qI_C}(C_{te} + C_{tc}) + \tau_b + \tau_E + \frac{W_{CB}}{2V_{sat}} + r_C C_{tc} \quad (1)$$

$$f_T = \frac{1}{2\pi\tau_{EC}} \quad (2)$$

where $\tau_b = \frac{{W_b}^2}{\gamma D_n}$, is the base transit time, $\tau_E = \frac{1}{\beta_{ac}}\left(\frac{W_E}{S_{pe}} + \frac{{W_E}^2}{2D_{pe}}\right)$ is the emitter transit time, C_{te}. and C_{tc} are the emitter-base and collector-base depletion capacitances, respectively, $W_{CB}$is the collector-base depletion region width, V_{sat} is the electron saturation velocity, W_b is the quasi-neutral base width, D_n is the electron diffusivity and r_C is the collector resistance. The quasi-electric field due to germanium grading in the base is included in the expression through the term $'\gamma'$.

To reduce the total transit time, primarily, the base and collector transit times are scaled. To reduce the base transit time, the base width is reduced through the use of aggressive thermal budgets. A thinner base also allows for increased peak germanium fraction for the same film stability which helps reduce the base transit time through increased quasi-electric field. The collector transit time is reduced through the use of increased collector doping concentration which reduces the width of the collector-base depletion region. The increased collector doping also helps delay high injection effects thereby allowing for a further reduction in capacitive transit time through increased collector current.

The vertical scaling strategy described above optimizes the intrinsic performance (f_T) of the bipolar transistor, which is relatively independent of the horizontal dimensions. The f_{max} of the transistor, however, is highly sensitive to parasitic elements and is therefore affected by horizontal scaling. The f_{max} of a bipolar transistor represents the maximum RF power gain of the transistor under matched conditions. It can be expressed as:

$$f_{max} = \sqrt[2]{\frac{f_T}{8\pi R_b C_{tc}}} \qquad (3)$$

where R_b is the base resistance of the HBT. The f_{max}, as seen from (3) is highly sensitive to the base resistance and collector-base capacitance which tend to degrade with vertical scaling. A thinner base helps minimize the base transit time and improves f_T, but also increases the base sheet resistance; this degrades the f_{max} of the transistor. Also, higher collector doping increases the collector-base depletion capacitance which further degrades f_{max}. To achieve a simultaneous improvement in f_T and f_{max} therefore, along with vertical scaling, the transistor is horizontally scaled by using finer lithography for the emitter window; this reduces the intrinsic base resistance and the area of the collector base capacitance and improves f_{max}. Second generation SiGe HBT's for example, employ a smaller base width (40 nm vs 65 nm), larger peak germanium concentration (25 % vs 10 %), higher collector doping, and a narrower lithography (0.18 μm vs 0.35 μm) as compared to a first generation device to achieve an improvement in both f_T and f_{max}..

A similar vertical and horizontal scaling strategy is employed for the transition from a second generation to a third generation device. However, in this case, additional structural modifications were found to be necessary for optimizing f_{max} [11]. The structure of a third

generation SiGe HBT is shown in Figure 2. The first and second generation HBTs employ a self-aligned implanted extrinsic base to reduce the base resistance. This scheme, however, was found to be inadequate for increasing the f_{max} of the transistor to 200GHz [11]. This was because, the defects created by extrinsic base ion implantation leads to excess base dopant outdiffusion leading to base widening and the highly doped, extrinsic base-SIC junction adds a large parasitic capacitor to the intrinsic collector-base capacitance. To avoid this performance limitation, the extrinsic base structure for the third generation device is modified from a self-aligned extrinsic base to a raised extrinsic base structure. This removes the highly doped extrinsic base from the vicinity of the collector-base junction thereby eliminating the extrinsic parasitic junction.

The fourth generation SiGe HBT, is a vertically scaled version of the third generation device with a few additional structural modifications.

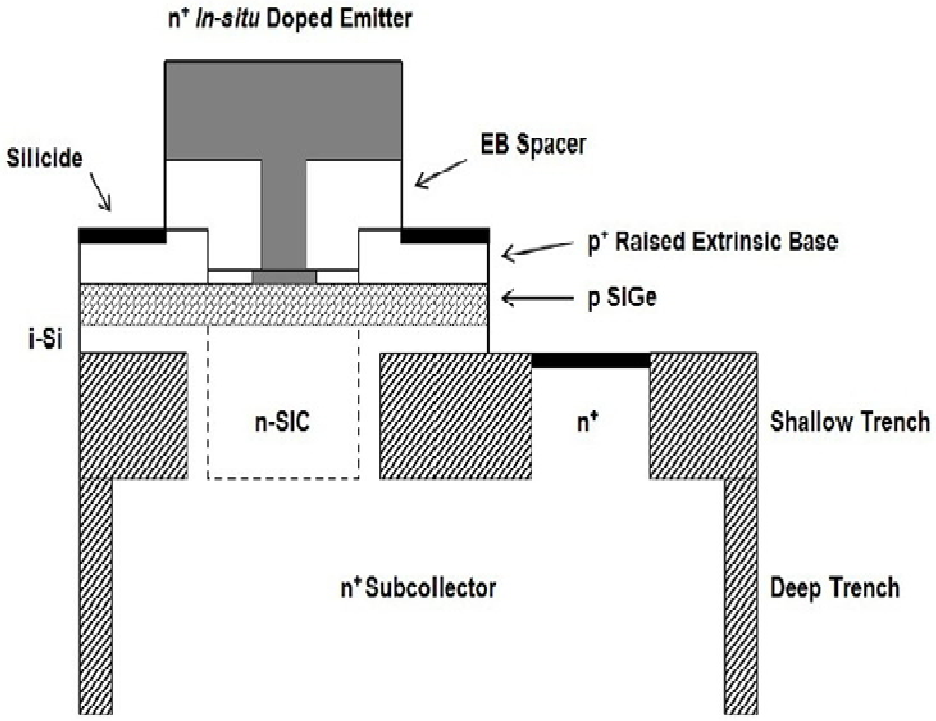


Figure 2. Structure of a third generation SiGe HBT

1.4 SiGe HBTs for EE Applications

While the performance of SiGe HBTs in the analog and RF domain is impressive, their capabilities in extreme environments is equally, if not more, impressive. Exposure to cryogenic temperatures improves the performance of SiGe HBTs and SiGe HBTs have also been proven to be immune to high levels of TID damage with various radiation particles. This potent combination of radiation hardness and cryogenic capabilities makes these devices especially suitable for extreme environment applications.

1.4.1 Cryogenic Performance of SiGe HBTs

The bandgap engineered nature of SiGe HBTs implies that many of important performance metrics of a SiGe HBT improve with cooling. The improvement in current gain of a SiGe HBT (assuming a triangular germanium profile and constant base doping) over an identically designed silicon BJT can be expressed as [2]:

$$\frac{\beta_{SiGe}}{\beta_{Si}} = \frac{\frac{\gamma\eta\Delta E_{g,Ge(grade)}}{kT} e^{\frac{\Delta E_{g,Ge(0)}}{\mathrm{kT}}}}{1-e^{\frac{\Delta E_{g,Ge(grade)}}{kT}}} \qquad (4)$$

where $\Delta E_{g,Ge(grade)}$ is the bandgap difference between the emitter and collector end of the base due to germanium grading and $\Delta E_{g,Ge(0)}$ is the bandgap reduction at the emitter base junction due to germanium. As seen from (4), a reduction in thermal voltage due to cooling increases the benefit of Germanium. The improvement in current gain of a third generation SiGe HBT with cooling is illustrated in Figure 3. The current gain at medium injection improves monotonically with reducing temperature as predicted by (4).

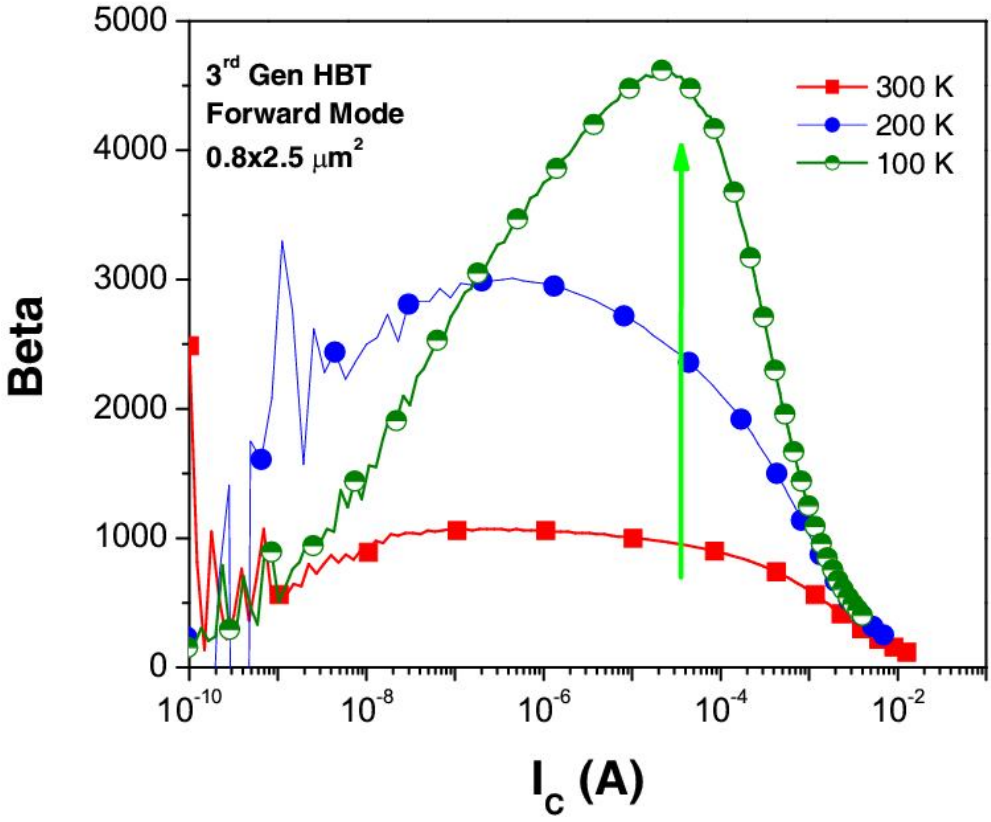


Figure 3. Forward mode current gain as a function of collector current

Cryogenic temperatures also enhance the dynamic performance of SiGe HBTs as can be derived from (1). The saturation velocity and mobility are enhanced while the depletion capacitances decrease with cooling. The electric field due to bandgap grading in the SiGe base is also enhanced at lower temperature. All transit time components are therefore reduced with cooling, thereby, improving the f_T of the transistor. Since SiGe HBTs are heavily doped, freezeout does not play a significant role in modulating the base resistance of the device. Combined with the improved hole mobility at cryogenic temperatures, the base resistance is reduced at lower temperatures which improves the f_{max} of the device. Peak f_T and f_{max} for SiGe HBTs have been shown to improve monotonically with cooling to greater than 500 GHz at 4.2 K [12, 13].

1.4.2 TID Response

SiGe HBTs have repeatedly been shown to be total ionizing dose hard up to a few Mrads of total accumulated dose for a variety of ionizing species [14]. The TID hardness of as-built SiGe HBTs arises out of the high doping employed in the device which minimizes the effect of accumulated charge in the spacer and STI oxides. SiGe HBTs are also immune to displacement damage effects due to their small device volume which limits the potential volume of interaction with the ionizing species.

1.5 Scaled CMOS Devices for EE Applications

One of the major advantages of SiGe HBT technology is that it can be integrated with state-of-the-art CMOS technology for a true system-on-a-chip integration. It is therefore important that along with SiGe HBTs, which have been shown to perform well in EE's, scaled CMOS devices are also examined for their performance in extreme environments.

1.5.1 Cryogenic Performance of Scaled CMOS Devices

The advantages of low temperature operation of MOSFETs have been known for a long time [15]. Decreasing temperature improves the mobility and saturation velocity of charge carriers in the channel leading to improved transconductance, and drain current. A reduction in source/drain series resistance with cooling further aids the improvement in intrinsic device performance. Also, a steeper subthreshold slope at lower temperature reduces the subthreshold leakage. In addition, off-state leakage currents like gate-induced-drain-leakage are thermally activated and become negligible at cryogenic temperatures.

Shown in Figure 4 are the transfer characteristics of a 80 nm drawn gate length bulk n-MOSFET as a function of temperature. As expected, the drive current increases monotonically with lower temperature. The subthreshold slope improves from 89 mV/decade at 300K to 29 mV/decade at 100 K. The off-state leakage for these devices does not, however, decrease with cooling since it is dominated by temperature independent gate direct tunneling into the source/drain extensions.

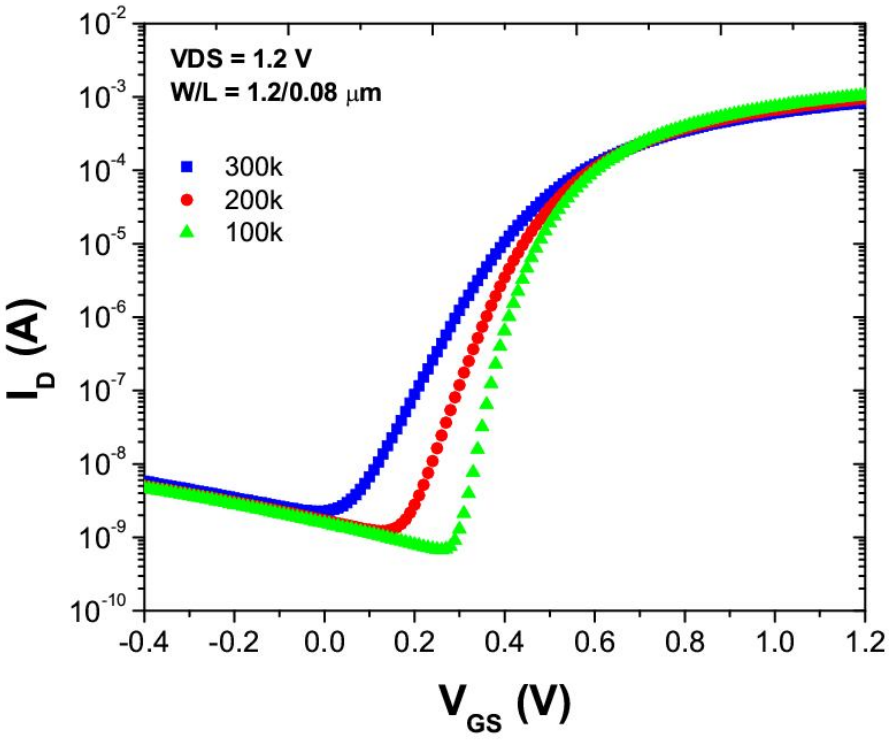


Figure 4. Transfer characteristics of 80 nm gate length nMOSFET at different temperatures

In Figure 5, the normalized peak transconductance of nMOSFETs of multiple gate lengths from a 90 nm bulk technology node is plotted as a function of temperature. The transconductance is normalized to the value at 300K. As expected, the transconductance improves significantly with lower temperature. The improvement in transconductance is higher for devices with a larger gate length since devices with a smaller gate length have a higher

effective channel doping due to halo implants and their mobility therefore is limited by Columbic scattering.

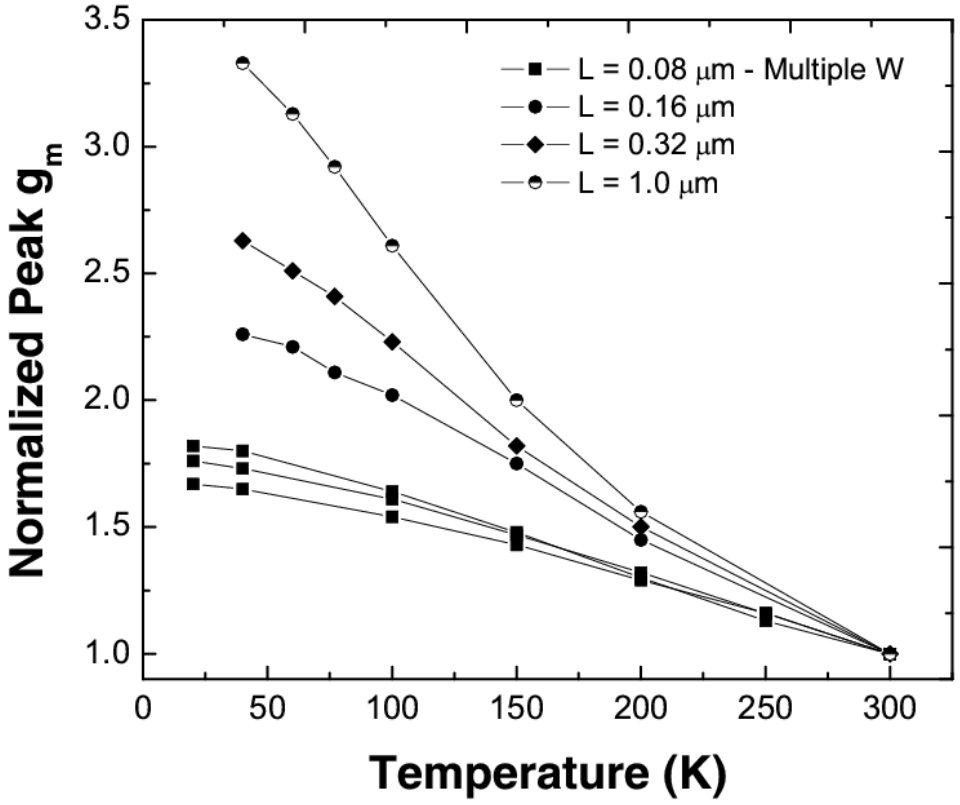


Figure 5. Normalized peak transconductance as a function of temperature for device of different gate lengths

1.5.2 Radiation Response of 90 nm CMOS Technology

While the improvement of MOSFET performance with cooling is beneficial for EE applications, MOSFETs, classically, were highly vulnerable to total ionizing dose effects [5]. With decreasing gate oxide thicknesses however, MOSFETs have become increasingly immune to total ionizing dose damage [16] since the ultra-thin gate oxides employed in sub-100nm MOSFETs do not contain enough volume for fixed charge storage.

Advanced MOSFET nodes also employ strain engineering as an integral part of device design for performance improvement [17]. While a significant amount of research has addressed the effects of radiation on conventional CMOS devices [16, 18], the effects of radiation on strained-silicon CMOS devices has not been previously reported [45]. In particular, although the improved intrinsic tolerance of conventional CMOS devices to ionizing radiation damage with scaling is well-established, the effect of displacement damage on the induced mechanical strain in strained-silicon devices has not been investigated. Here, we demonstrate the TID tolerance of a strained-silicon CMOS technology built on SOI.

The device technology investigated is a 90 nm drawn gate length, PD-SSOI technology, with a drawn gate length (L_{poly}) of 45 nm, a gate width (W) of 7.0 μm, and a gate oxide thickness (t_{ox}) of 1.2 nm. The devices were designed in H-Gate (edgeless) topologies with two body contacts. The strain was applied uniaxially to the channel using nitride spacers, as depicted in Figure 6. The devices were built on a UNIBOND SOI wafer with a buried oxide thickness of 140 nm. In this experiment only the pFETs were strained. The device technology has been described in greater detail in [19, 20] and was not radiation-hardened in any way.

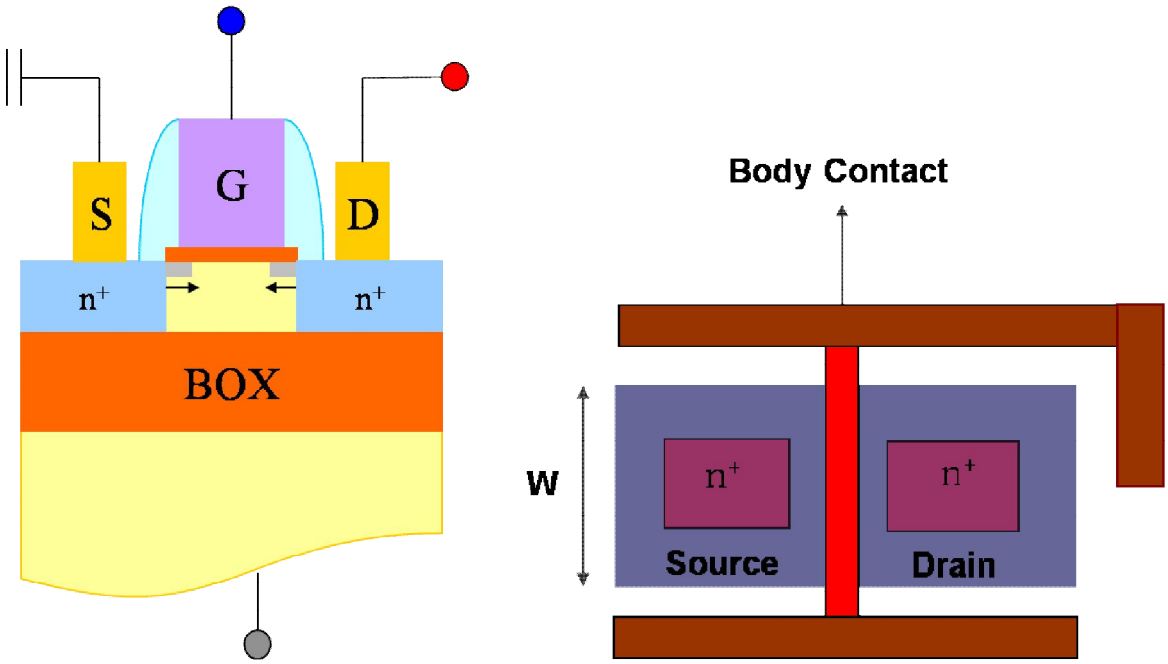


Figure 6. Structure of a 90 nm partially depleted strained silicon on insulator MOSFET. The device employs H-gate topology with two body contacts

Typical transfer characteristics for the strained-silicon pFETs are shown in Figure 7, along with those for an unstrained control device for direct comparison. The devices have identical subthreshold swings of 85 mV/decade and the extracted threshold voltages (defined at a constant current of 0.1 μA/μm) are -0.25V and -0.19V for the strained and unstrained devices, respectively. The slight difference in threshold voltage for the two devices can be attributed to slight (unintended) differences in processing. From the slope of the drain current (I_D) in the linear transfer characteristics shown in Figure 7, one can clearly see the strain-induced improvement in effective mobility. The extracted values of the low field mobility (extracted using the techniques in [21]) for the strained and unstrained pFETs are 53.9 and 40.3 cm^2/V-s, respectively. The extracted mobility for the nFET is 197 cm^2/V-s. The improvement in mobility for the strained pFET translates to a 29% improvement in the output drive current at a gate

voltage (V_G) of -1.0 V, after taking into account the difference in threshold voltage between the two devices.

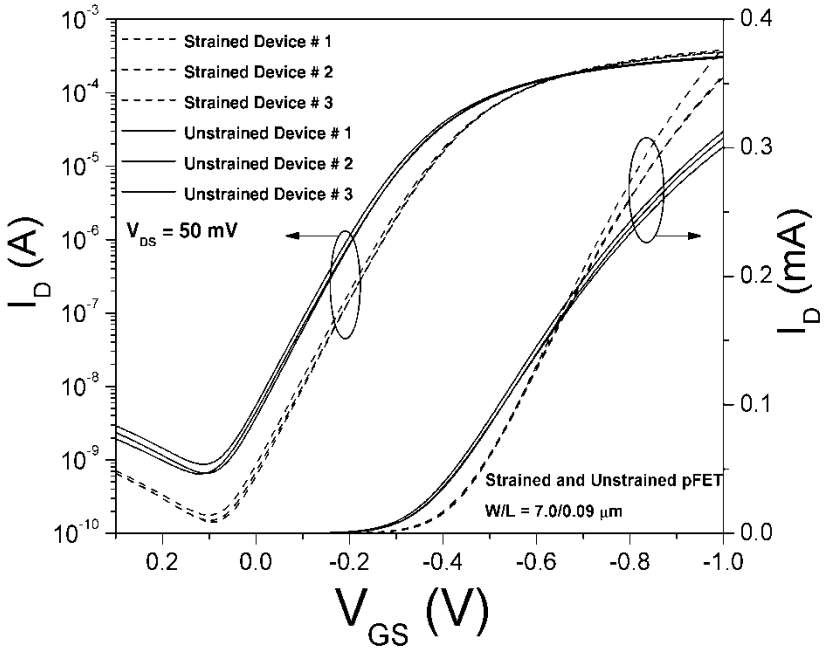


Figure 7. Transfer characteristics of strained and unstrained pFETs

For irradiation, the devices were wire-bonded into 28-pin DIP packages and exposed to 63 MeV protons at a dose rate of 1.0 krad(Si)/sec at the Crocker Nuclear Laboratory [22] at the University of California at Davis (note: 1.00 rad(SiO_2) = 1.05 rad(Si) for 63 MeV protons). All pins were grounded during exposure and measurements were performed *in-situ* immediately after each dose point was reached, using standard measurement protocols. Dosimetry measurements used a five-foil secondary emission monitor calibrated against a Faraday cup. The radiation source (Ta scattering foils) was located several meters upstream of the target to establish a beam spatial uniformity of about 15 % over a 2.00 cm radius circular area. Beam currents from about 20 to 100 nA allowed testing with proton fluxes from $1.0x10^9$ to $1.0x10^{12}$ protons/cm^2-sec. The dosimetry system is known to be accurate to about 10%. The proton

fluence was increased to achieve a varying equivalent total dose ranging from 20 krad(Si) up to a maximum of 600 krad(Si). Additionally, the devices were exposed to 4 MeV protons at a dose rate of 1 krad/sec at the Accelerator Laboratory of Auburn University. Hydrogen beam currents of approximately 20 nA from a 2 MeV tandem Pelletron accelerator equipped with a SNICS II source was used. The beam current was measured using a biased National Electrostatics Corporation Faraday cup. Beam uniformity is known to be accurate to about 12% over an irradiated circular target area of radius 2.5 cm.

Typical front-gate characteristics and the transconductance (g_m) for the nFETs and the pFETs are shown in Figures 8 and 9, respectively. The devices did not show any degradation in performance after 63 MeV proton irradiation, up to the equivalent maximum dose of 600 krad(Si). This is extremely encouraging, since it demonstrates the robustness of the process-induced strain to any displacement damage associated with proton exposure.

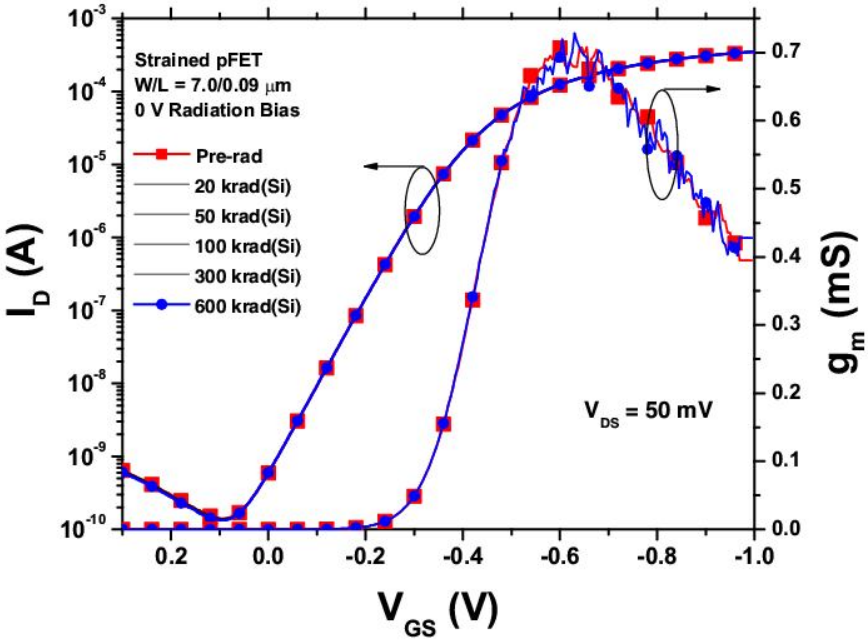


Figure 8. Transfer characteristics and gm of the strained pFET as a function of dose.

An examination of the unstrained device characteristics (not shown here for brevity) gives identical results (i.e., essentially no radiation-induced degradation). In addition, the front-gate characteristics of the nFETs do not reveal any enhanced leakage due to the charge collection in the back gate, a known potential problem with standard SOI CMOS devices.

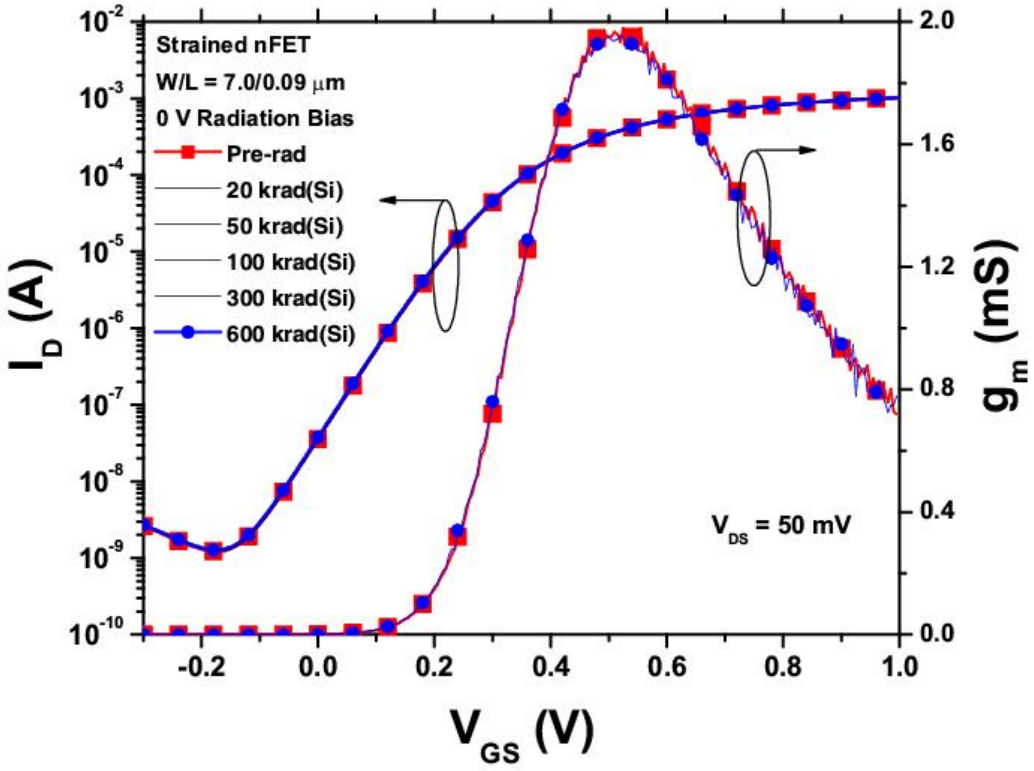


Figure 9. Transfer characteristics and gm of the unstrained nFET as a function of dose.

An examination of the nFET back-channel characteristics shows an expected significant change in the back-gate threshold voltage, but remains acceptably high for the maximum dose used (Figure 10). For the pFET, the shift in the threshold voltage is significantly smaller and is due to the negative bias applied to the gate during measurements (Figure 11). Moreover, the threshold voltage shifts to higher substrate voltages and is therefore not a cause for concern for

increased parasitic leakage. The shift in threshold voltage with radiation dose is shown in Figure 12 for both the pFETs and the nFETs. These results for the back-gate radiation response are qualitatively consistent with previously reported data for an earlier generation standard SOI CMOS technology [16].

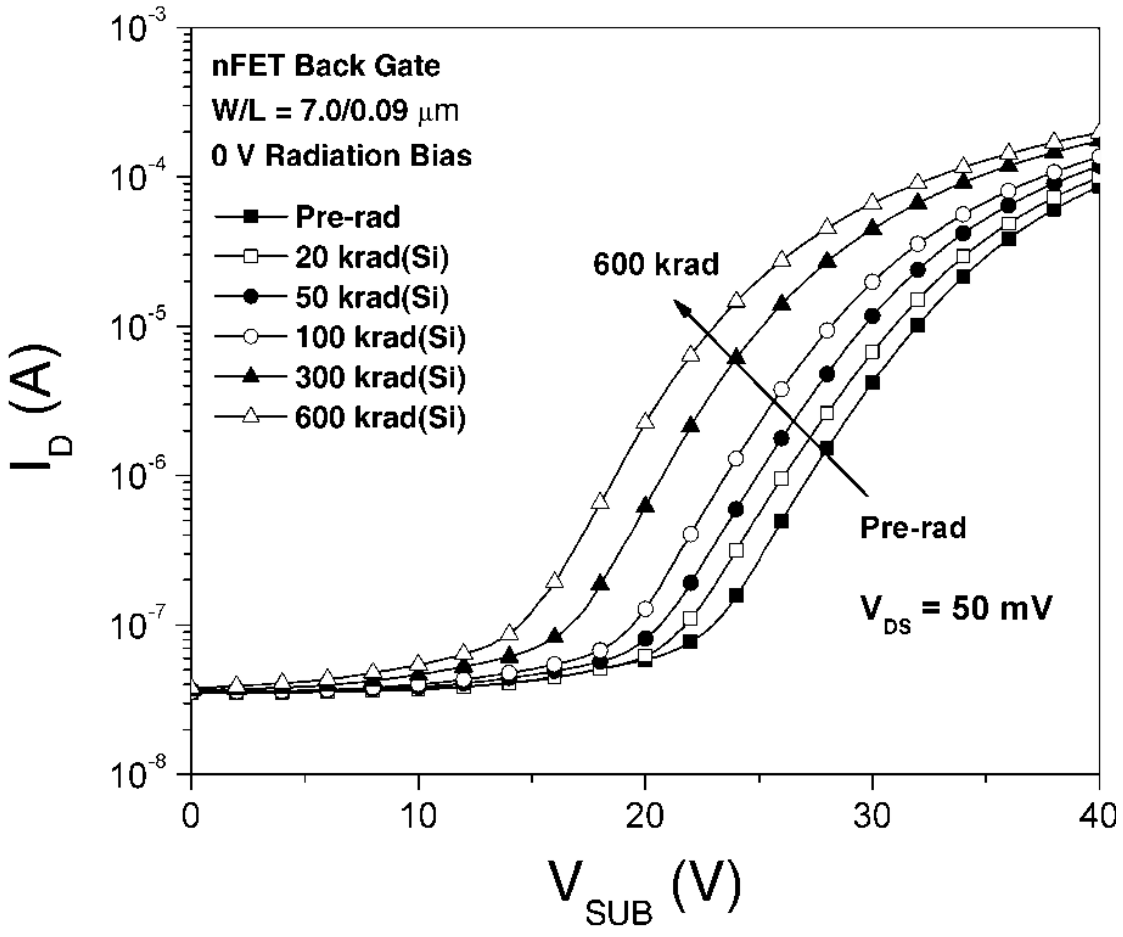


Figure 10. Back gate transfer characteristics of 90 nm nFETs as a function of dose

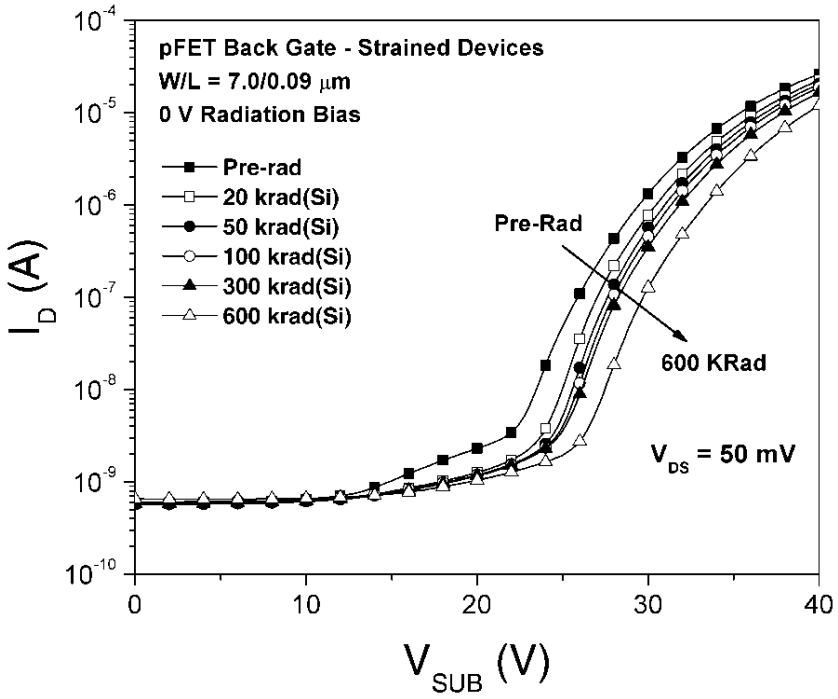


Figure 11. Back gate transfer characteristics of 90 nm pFETs as a function of dose

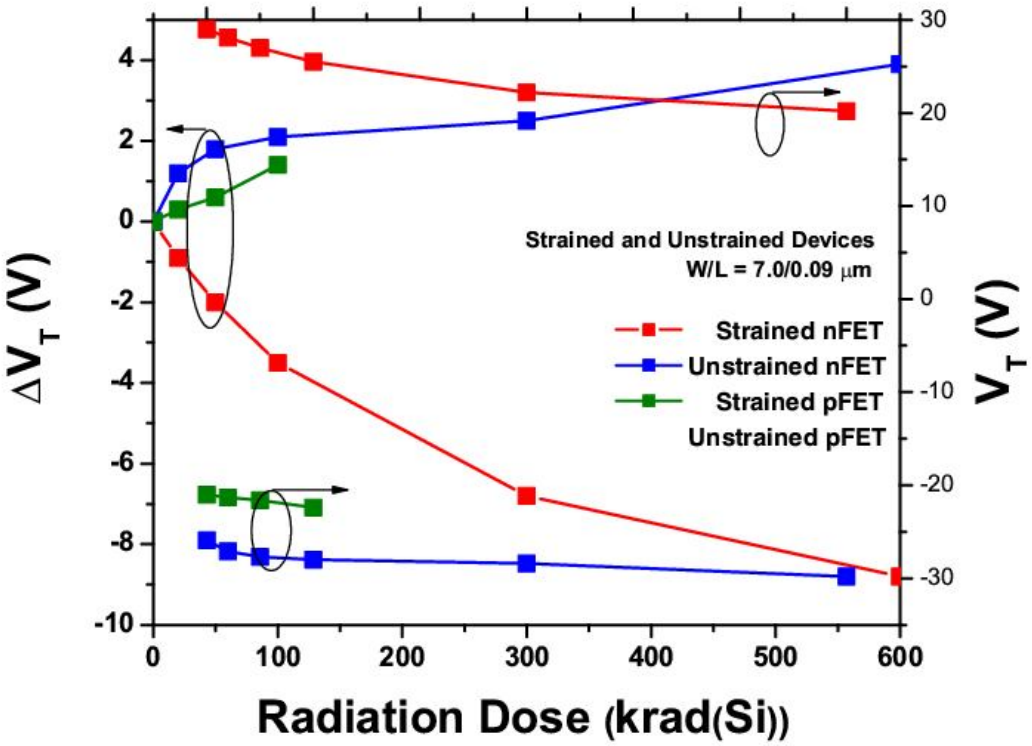


Figure 12. Back gate threshold voltage and threshold voltage shift as a function of dose for strained and unstrained nFETs and pFETs.

The devices were also passively exposed to low-energy (4 MeV) proton radiation up to 2 Mrad to check for displacement damage. As can be seen in Figure 13, the devices do not show any signs of displacement damage and are radiation hard even to highly damaging low energy protons. The strained pFETs (not shown here) also did not show any noticeable change after 1 Mrad(Si) of 4 MeV proton irradiation.

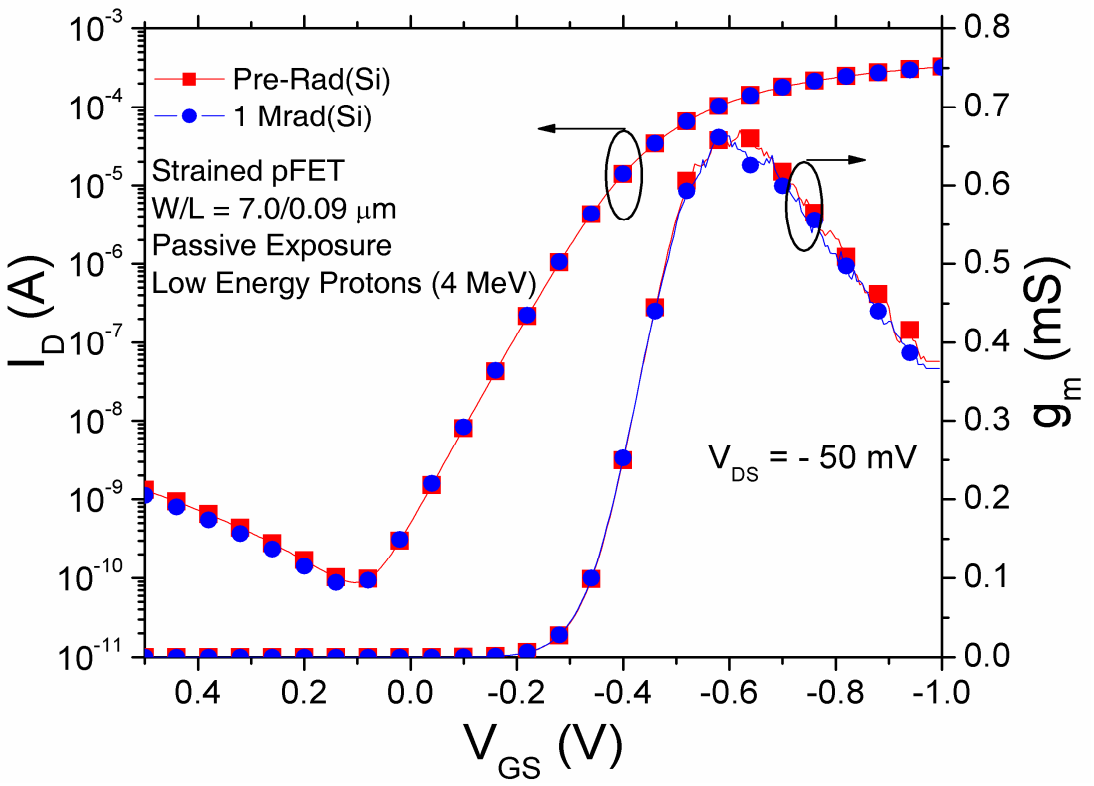


Figure 13. Transfer characteristics for unstrained pFET after 2 Mrad(Si) of low energy (4MeV) proton exposure.

These results are extremely encouraging and address one aspect of potential concern for operation of CMOS in extreme environments.

Chapter 2

Inverse Mode Operation of SiGe HBTs

In chapter 1, SiGe HBTs were introduced as a viable candidate for extreme environment applications. In this chapter, the vulnerability of SiGe HBTs to single event effects is discussed and the inverse mode operation of SiGe HBTs is introduced as a SEU-hard solution. Further, the impact of scaling on inverse mode performance of SiGe HBTs is discussed. The results discussed in this chapter have been published in [46, 47].

2.1 Single Event Effects

While SiGe HBTs have been proven to be tolerant to TID effects, SiGe HBT circuits have been shown to be vulnerable to single event upsets even at low linear energy transfer (LET) values [23]. The sensitivity to single event upset is not just limited to silicon bipolar technology, but is a key limitation of any unhardened bulk technology (either bipolar or CMOS) in space-based applications [24, 25, 26]. The susceptibility of bulk technology to SEU's necessitates expensive process-based and/or circuit-based radiation hardening, leading to an undesirable cost/power/performance tradeoff.

In semiconductor devices, SEU's are caused by highly energetic particles passing through the silicon lattice. The electron hole pairs created in the path of the energetic particle are separated by the electric fields present in the device regions and are collected at the various device terminals. In bipolar transistors, of particular importance in the context of SEU is the collector-substrate junction and the quasi-neutral substrate region since these two device regions hold the maximum semiconductor volume and hence collect the maximum charge.

A representative ion strike on a SiGe HBT is illustrated in Figure 4. In a typical circuit application, the collector-substrate junction is reverse biased. During an ion strike, the large number of electron hole pairs created by the incident charge particle changes the electrostatics of the collector-substrate junction. The excess electron-hole pairs cause a collapse of the collector-base junction field and the reverse bias across the collector substrate junction is subsequently supported by the quasi-neutral bulk collector-substrate regions. The electric field generated in the quasi-neutral substrate accelerates the holes towards the substrate terminal while simultaneously driving the electrons towards the collector terminal. The drift field persists till the excess carriers are removed from the device as terminal currents or by recombination.

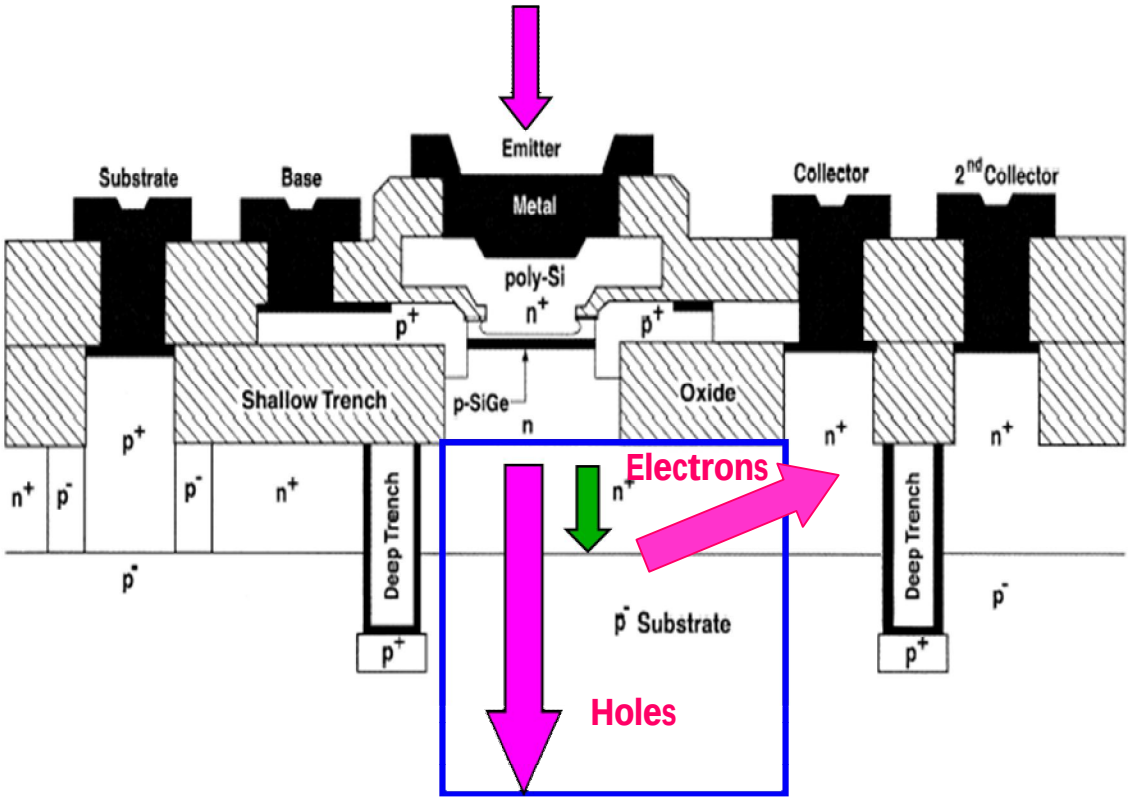


Figure 14. SEU mechanism in SiGe HBTs

Shown in Figure 15 is the measured charge collection profile from a heavy ion strike (in this case for a 36 MeV oxygen ion) for a 3rd generation, SiGe HBT as a function of the location of the heavy ion strike. The experimental setup for these heavy ion-induced charge collection measurements is fully described in [27]. The device was operated during irradiation with a large reverse bias across the collector-substrate junction, as would be experienced in circuit operation, to maximize charge collection; all other terminals are grounded. Electron-hole pairs (EHPs), most of which are created in the substrate, diffuse to the collector-substrate junction, and are predominantly collected at the substrate and collector terminals of the transistor. The emitter and base charge collection, however, fall below the resolution of the measurement. It is to be noted that the deep trench isolation dramatically reduces the charge collected from an ion strike that occurs outside of the device area.

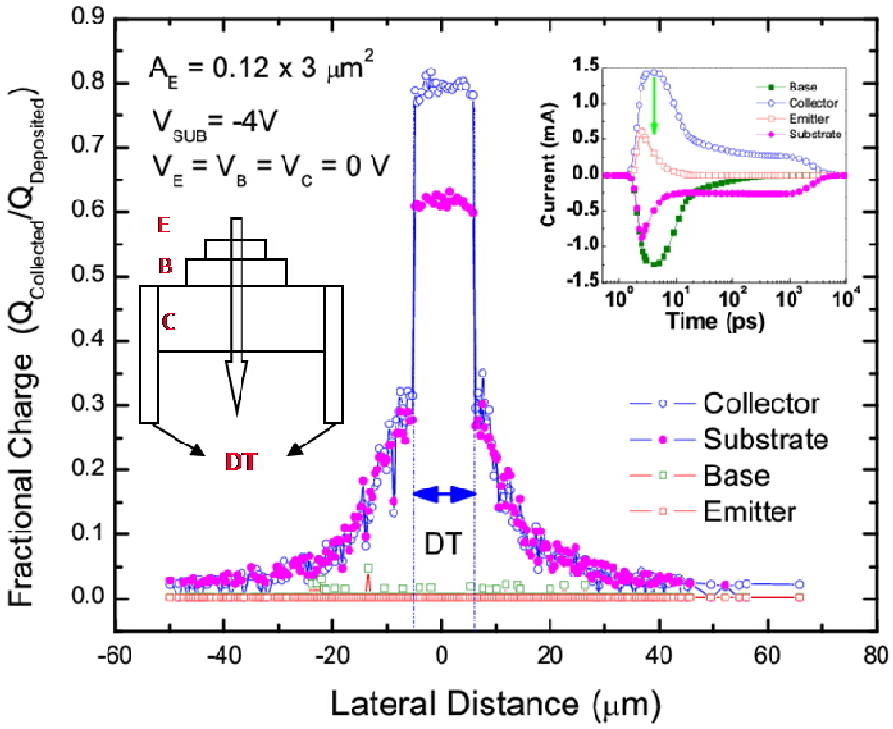


Figure 15. Charge collection in various terminals in a third generation SiGe HBT exposed to oxygen ions

The charge collected at the collector terminal is a cause for concern since the collector terminal is usually the output terminal for the transistor. For example, shown in Figure 16, is a schematic of a simple differential pair that forms an integral part of many basic analog and digital circuit blocks. Assuming that the transistor on the left is biased to be non-conducting, a SEU strike on that transistor would inject a pulse of current into its collector terminal which changes the state of its output from low to high. This error due to the ion strike propagates along a shift register causing bit errors.

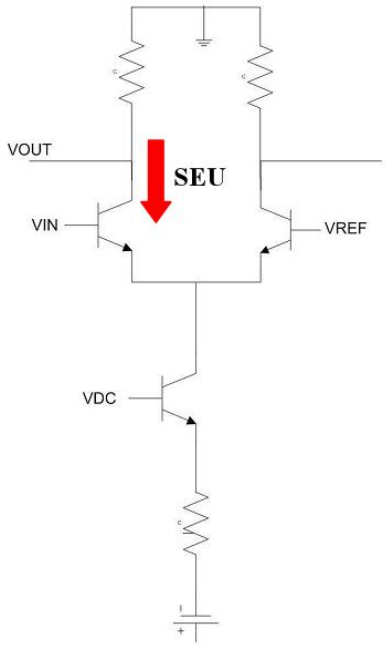


Figure 16. Schematic diagram of a forward mode differential pair. An ion strike causes upsets in the 'off' transistor

2.2 Inverse Mode Operation for SEU Mitigation

As discussed previously, the errors due to the ion strike arise fundamentally due to the coupling of the output terminal of the transistor (collector) with the charge collecting substrate region. At a device level, this coupling can be avoided by biasing the transistor in the inverse mode of operation as shown in Figure 17. In the inverse mode of operation, the bipolar transistor is biased to electrically swap the collector and emitter terminals. The physical collector of the transistor, in inverse mode, acts as the electrical emitter and vice versa. Since the electrical collector in inverse mode is decoupled from the charge collecting substrate terminal, the current transients in the output node can be mitigated. An examination of the charge collection characteristics of a third generation SiGe HBT, shown in Figure 15, confirms this; the physical emitter of the HBT collects negligible charge from the ion strike. In inverse mode, the physical emitter would constitute the output node and the circuit would, therefore, not cause a bit error.

Another important figure-of-merit for assessing the SEU tolerance of digital circuits is the collector current transient generated during the heavy ion strike, since that output current transient can flip the voltage at the output node in CML/ECL bipolar digital circuits employing forward-mode devices, causing bit errors (SEU) (Figure 16). Calibrated 3-D TCAD simulated current transients due to the heavy ion strike are shown in the inset of Figure 15. As can be seen, the ion-induced current transient at the emitter terminal is 50% smaller than the transients at the collector terminal, and the duration of the transient is dramatically reduced from a few nanoseconds at the collector to a few picoseconds in the emitter. An additional advantage in using a collector-up structure is the reduction in (vulnerable) electrical collector-base junction area, which further adds to the single event immunity.

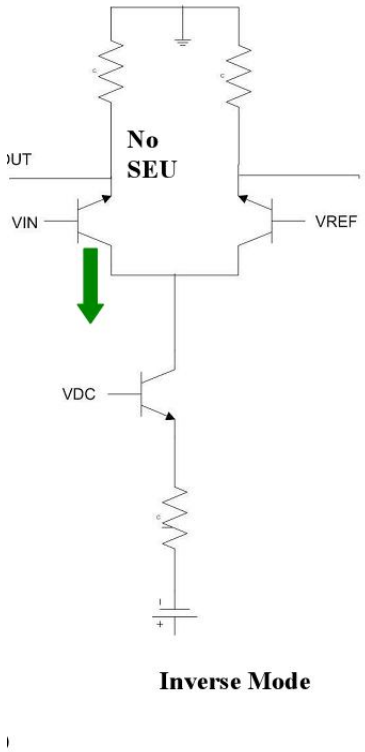


Figure 17. Schematic of an inverse mode SiGe HBT differential pair. The charge due to ion strike is isolated from the output node of the transistor

While the SEU tolerance of inverse mode SiGe HBTs seems promising from a space-application perspective, historically, a serious impediment to the application of inverse-mode bipolar transistors for digital circuits, was their significantly degraded performance compared to their (intended) forward-mode operation. In the following section we examine the impact of scaling on the inverse mode operation of SiGe HBTs and examine the limitations of inverse mode performance of SiGe HBTs.

2.3 Inverse Mode Operation of SiGe HBTs

SiGe HBTs, like other bipolar technologies, are designed to operate exclusively in the forward mode of operation. Scaling strategies for SiGe HBTs have therefore been exclusively

focused on the forward mode of operation. However, as will be demonstrated, an auxiliary benefit of continued generational scaling has been the simultaneous improvement in the inverse mode (reverse mode) operational characteristics of SiGe HBTs.

In the silicon world, inverse mode of operation was used in the historically-important Integrated-Injection-Logic (I^2L), where the transistors are biased to operate in the inverse mode to achieve high density, low power digital logic [28]. The inverse mode operation of the then state-of-the-art transistors, however, suffered from a variety of limitations, and this particular digital family was subsequently supplanted by CMOS technology. With vertical and horizontal scaling however, the inverse mode performance improves (as will be demonstrated here) due to improved gain and reduced capacitances. The addition of germanium to the base of the BJT improves the collector current, and therefore, current gain in inverse mode and lateral scaling has resulted in significantly reduced capacitances. It is therefore logical to revisit the inverse mode performance of modern SiGe HBTs, to quantitatively assess the impact of generational scaling. Understanding the physics and limitations of inverse mode operation is also necessary to optimize the device for inverse mode performance.

The idea of a “symmetrical” bipolar transistor, in which the forward mode and inverse mode device characteristics are balanced, is not new. An optimized structure for symmetrical operation of HBTs was proposed by Kroemer in 1982 for the III-V material system [29], and devices optimized for the inverse mode (collector-up) operation have been demonstrated in several III-V materials (e.g., [30 - 33]). Inverse mode transistors in the III-V world, potentially offer improved performance over traditional forward mode emitter-up transistors due to their lower CB capacitance, and decreased coupling with the substrate. However, inverse mode performance has suffered in both the III-V and silicon world due to electron injection into the

extrinsic portion of the HBT, resulting in decreased ac performance due to charge storage in the extrinsic base. Various attempts have been made in the III-V world to overcome this limitation by either oxygen implantation or by etching away portions of the extrinsic collector with varied success [31 - 33]. In SiGe HBTs, the use of a selectively implanted collector (SIC) serves as a natural "confiner" of electron current density into the intrinsic portion of the device by increasing the resistance of the extrinsic portion of the physical collector. The SIC also reduces the physical collector-base capacitance.

The first SiGe HBT explicitly optimized for inverse mode operation was demonstrated by Burghartz [34]. The device used symmetrical doping in the emitter and the collector and showed impressive performance capabilities. A SiGe HBT structure optimized for inverse mode operation was also demonstrated by Gruhle [35]. Recently, J.-S. Rieh [36] examined the physics of inverse mode operation of SiGe HBTs and Kuo [37] reported, for the first time, inverse mode *ac* results on commercially-available SiGe HBTs. This work confines itself to commercially available SiGe HBTs for understanding the physics and to examine the impact of scaling on inverse mode performance, with the ultimate goal of suggesting optimized structures for inverse mode performance.

The devices investigated in this work represent four distinct generations of commercially compatible SiGe HBTs [7-10]. A schematic illustration of the structure of a first and third generation SiGe HBT along with the direction of electron flow in inverse and forward mode of operation of SiGe HBTs is illustrated in Figure 18. The second generation SiGe HBT shares a similar structure to the first generation device while the fourth generation device is a laterally scaled version of the structure of the third generation SiGe HBT. For reference, the distance between the shallow trench isolation (STI) edge and the edge of the selectively implanted

collector (SIC) region is larger for the second-generation device than for the first-generation device.

The measurements were done on a manual probing station using 4155C semiconductor parameter analyzer. Each measurement was repeated for multiple devices to ensure consistency of trends, and the data presented here are representative. Device simulations were performed with DESSIS [38]. The TCAD deck was initially calibrated to both DC and AC data for both the forward and inverse mode operation.

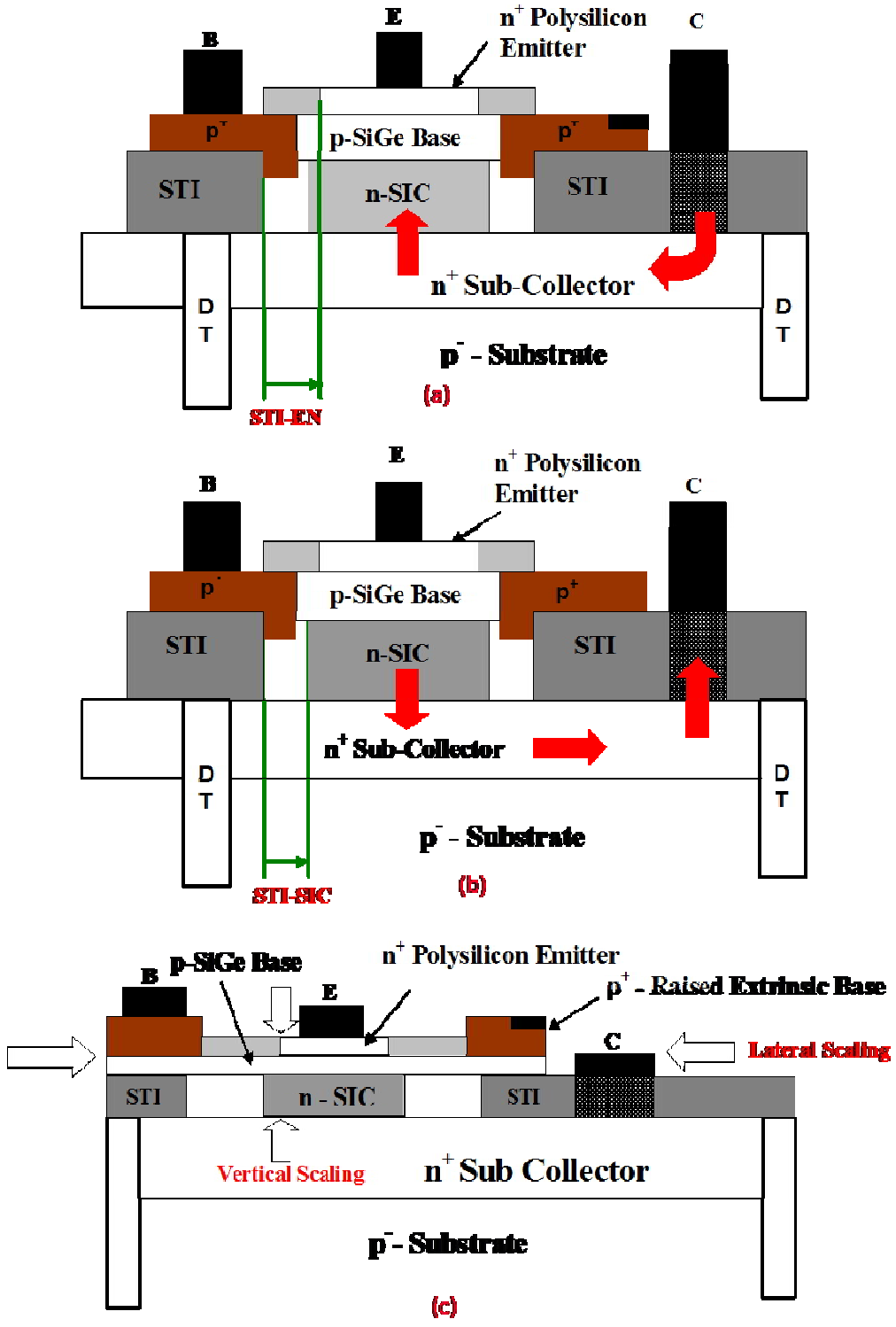


Figure 18. Structure of a first and third generation SiGe HBT. The electron flow path in inverse and forward mode are shown in (a) and (b) respectively. Scaling strategies for forward mode performance optimizations are shown in (c)

2.3.1 Scaling Effects

The forward mode Gummel characteristics for the four generations of SiGe HBTs are shown in Figure 19, where we plot the current densities (J_{CF}) for meaningful comparison across technologies. Device-to-device variations from the same SiGe generation have been measured to be well within the observed differences between technologies. A comparison of the forward mode current densities between the first- and second-generation devices reveals a large increase in the base (J_{BF}) and collector current density (J_{CF}) for the second-generation device due to a significant reduction in the emitter and the base Gummel numbers with scaling. The second- and third-generation J_{CF} values overlay, while the fourth-generation J_{CF} is increased even further by additional reduction of its base Gummel number.

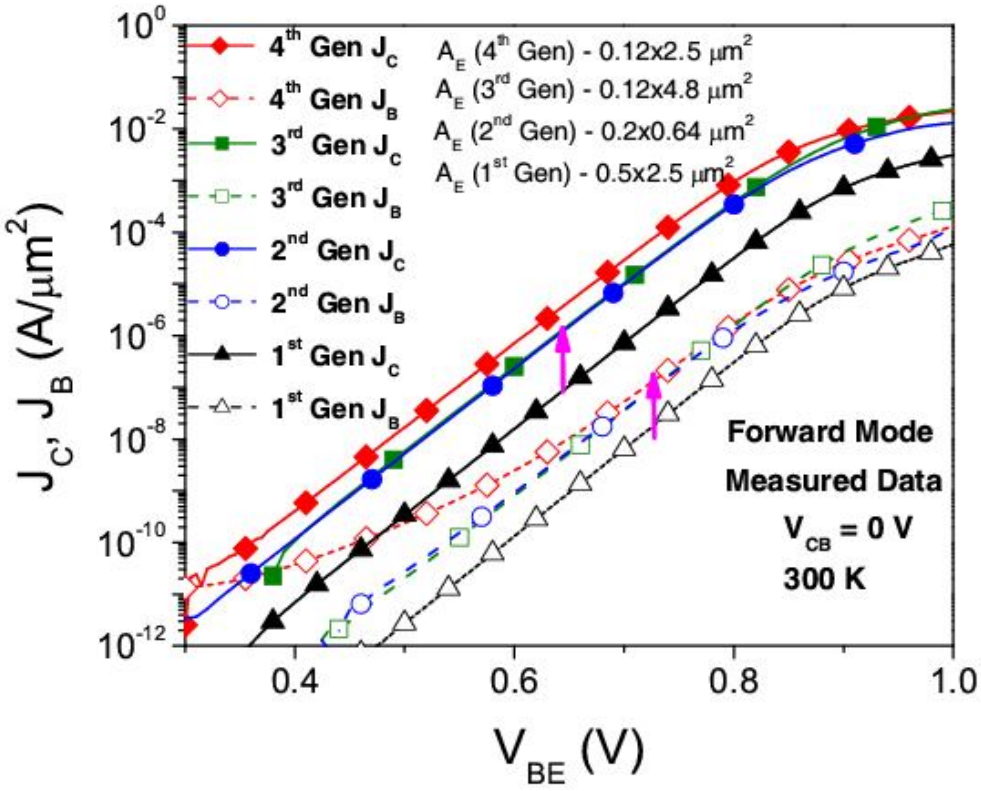


Figure 19. Forward mode Gummel characteristics for four generations of SiGe HBTs.

The scaling of SiGe HBTs has significant impact on their inverse mode performance, as illustrated in Figure 20, where we plot the inverse mode *dc* current gain (β) as a function of the inverse collector current density (J_{CREV}). The peak β monotonically increases from a value of about 12 for the first-generation devices, to a value of approximately 240 for the fourth-generation devices, clearly a dramatic improvement. It is significant that the improved current gain is a *natural* consequence of the forward mode performance optimization, and therefore does not require any special process modifications – clearly a significant advantage from a cost perspective. Previous literature on the inverse mode operation of SiGe HBTs [34, 35] investigated explicitly optimized structures for inverse mode performance improvement, and we note that in general, those devices were not compatible with existent commercial BiCMOS technology platforms. We now discuss the physics behind the observed improvement in the *dc* gain of standard SiGe HBTs with generational scaling.

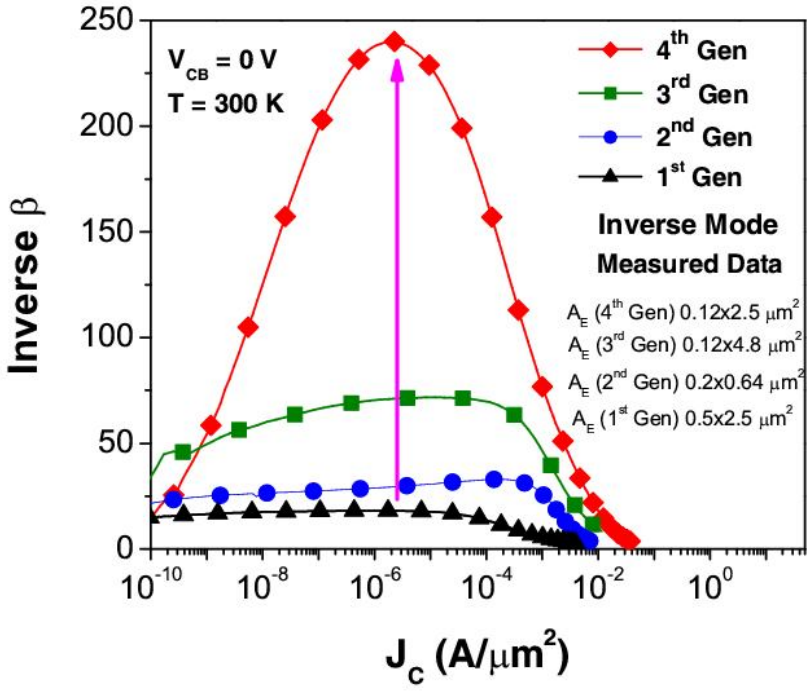


Figure 20. Inverse mode current gain for four generations of SiGe HBTs.

To determine if the gain improvement is a consequence of vertical scaling (due to increasing doping levels) of the physical collector, the inverse Gummel characteristics for devices that are optimized for either performance (f_T) or breakdown voltage (BV_{CEO}) were measured across all four technology generations. These devices differ only in their physical collector (SIC) doping profile, with an increased physical collector doping (N_C) used for improving the f_T and a reduced N_C profile used to trade f_T for higher BV_{CEO}. The inverse Gummel characteristics for the fourth-generation devices is plotted in Figure 21. One can observe from the data that while J_{CREV} is higher for the higher N_C device, the base current densities (J_{BREV}) in fact overlay. This dependence on N_C scaling is observed in the other three generations of devices as well, but for brevity, are not shown here. The increase in J_{CREV} for the higher performance devices is known to be due to the differences in base width between the high-performance and high-breakdown device. The observed SIC-doping-independent base current behavior, however, is unexpected, and to our knowledge not previously reported, and the underlying reasons for this behavior are now discussed.

To examine the effects of N_C on the inverse mode *dc* gain further, DESSIS simulations were performed with varying SIC doping concentrations for three generations of devices. Changing N_C by more than three orders of magnitude failed to produce any observable change in the simulated inverse mode base current (I_{BREV}). Furthermore, a comparison of the measured J_{BREV} between the first- and second-generation devices (Figure 22) reveals that the J_{BREV} is in fact significantly *higher* for the second generation device, contrary to what one would naively expect based on the doping profiles. The behavior of the third and fourth generation devices (Figures 23, 24) is examined later in this section.

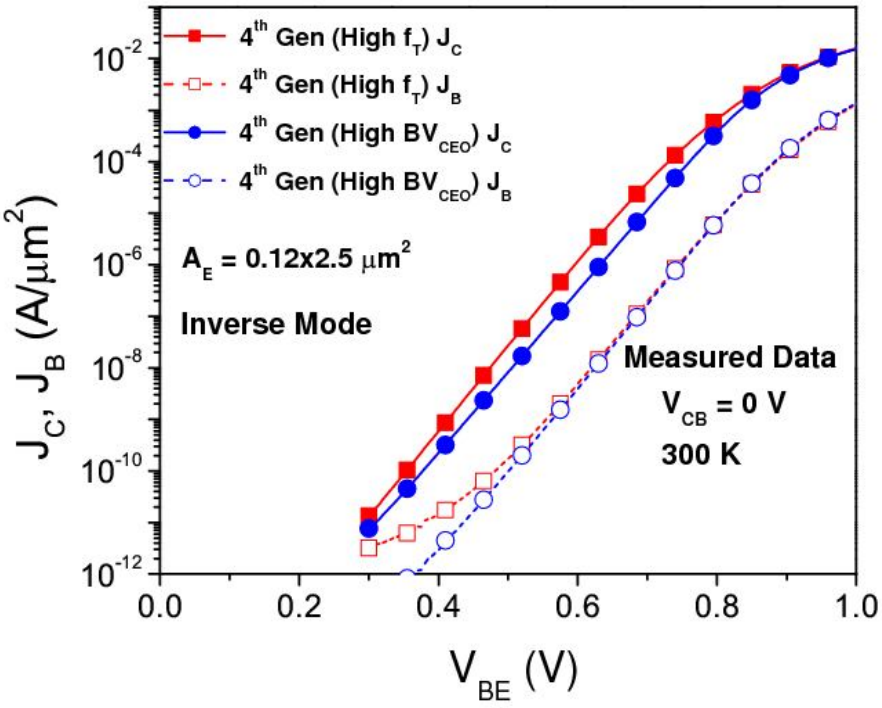


Figure 21. Inverse Gummel characteristics of a fourth generation SiGe HBT optimized for performance/breakdown voltage

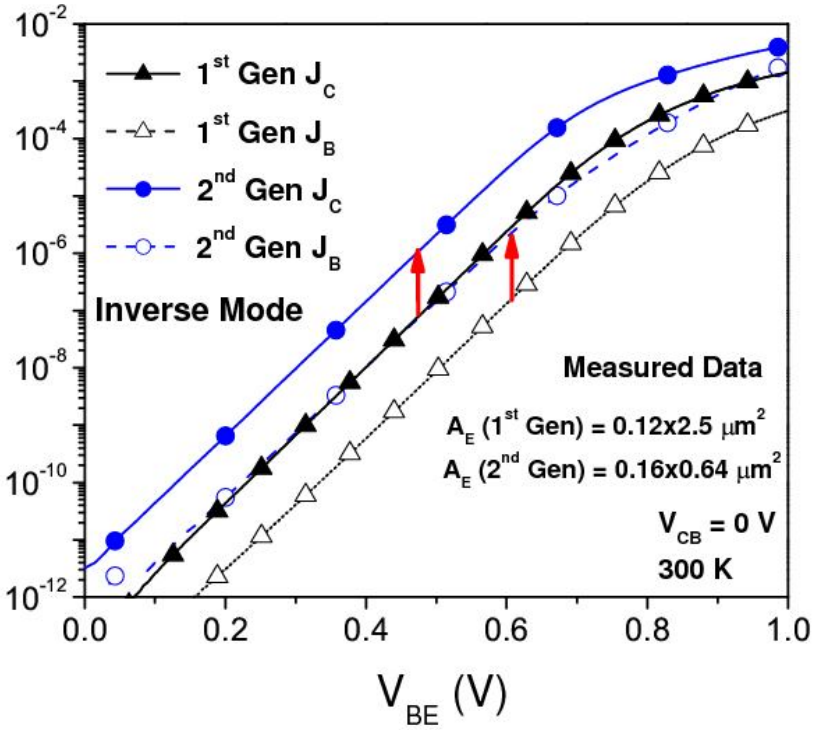


Figure 22. Inverse Gummel characteristics of first and second generation SiGe HBTs

(b)

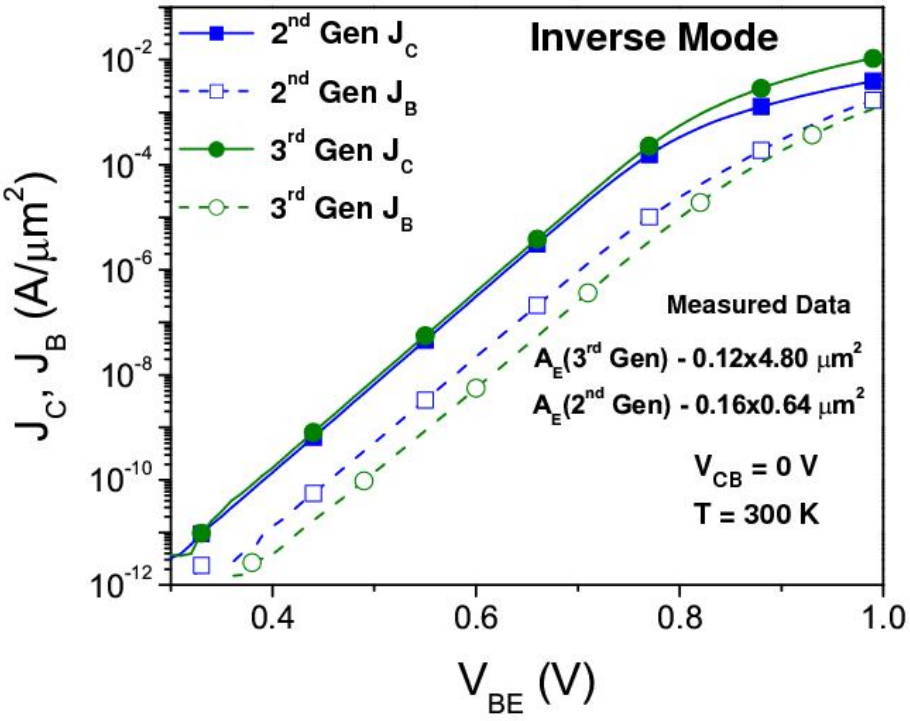


Figure 23. Inverse Gummel characteristics of second and third generation SiGe HBTs

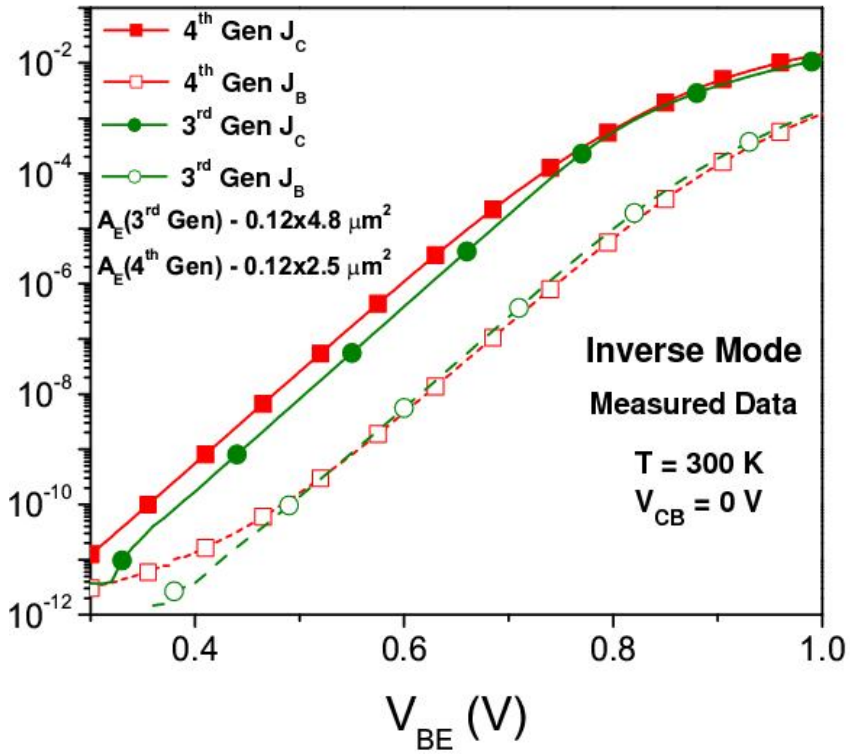


Figure 24. Inverse Gummel characteristics of third and fourth generation SiGe HBTs

The hole current distribution for the inverse mode at a V_{BE} of 0.6 V for a first-generation device is shown in Figure 25. As can be seen, I_{BREV} predominantly flows in the region outside the SIC region, between the SIC and STI edge. A simulation of the current flow for the second-generation device is identical and is not shown here for brevity. From the current distribution, one can conclude the following with respect to the inverse mode base current:

1) The area dominating the base current is not equal to the area dominating the collector current (which is equal to the area of the physical emitter - A_E [36]).
2) The magnitude of the base current should be proportional to the STI-SIC distance, because the STI-SIC distance defines the effective area for the dominant base current component.

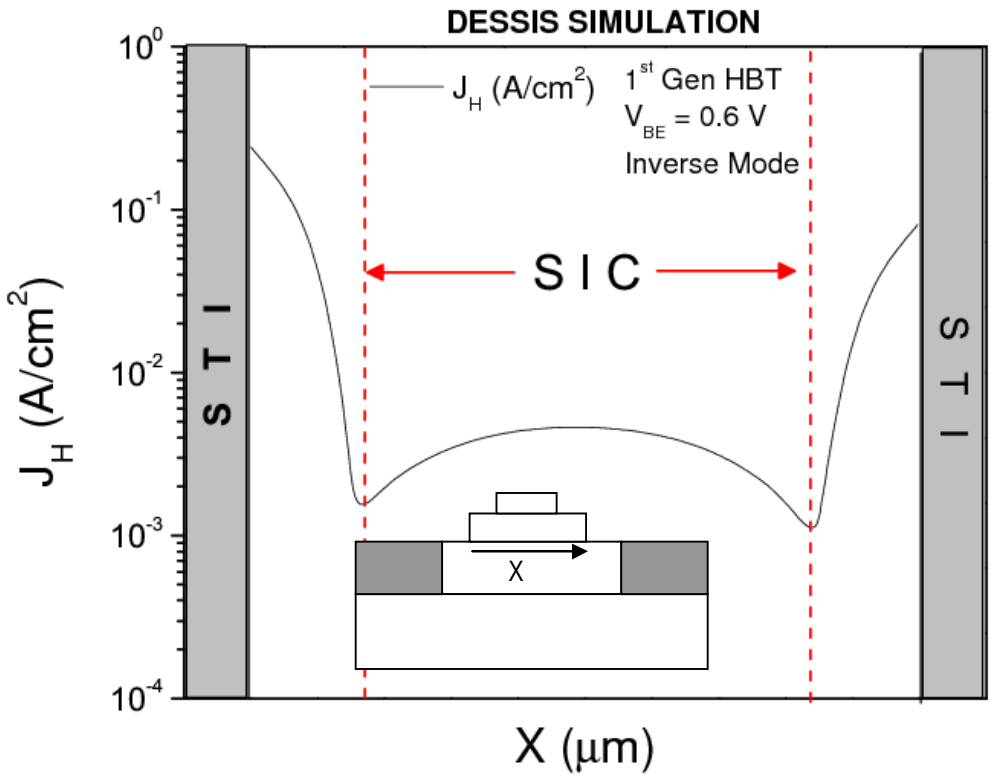


Figure 25. Inverse mode hole (base) current density distribution at V_{BE} = 0.6 V for a first-generation SiGe HBT.

To verify the above conjecture, the inverse Gummel characteristics for the first-generation device was simulated by scaling the device laterally, while keeping the STI-SIC distance and the doping profiles constant. One can observe in Figure 26 that I_{CREV} decreases as the lateral dimensions shrink (with W_E), while the base current remains constant. A plot of the current densities will therefore overlay J_{CREV}, but J_{BREV} will be shifted upward (made larger) for the smaller geometry device – similar to what is seen between the first- and second-generation device data.

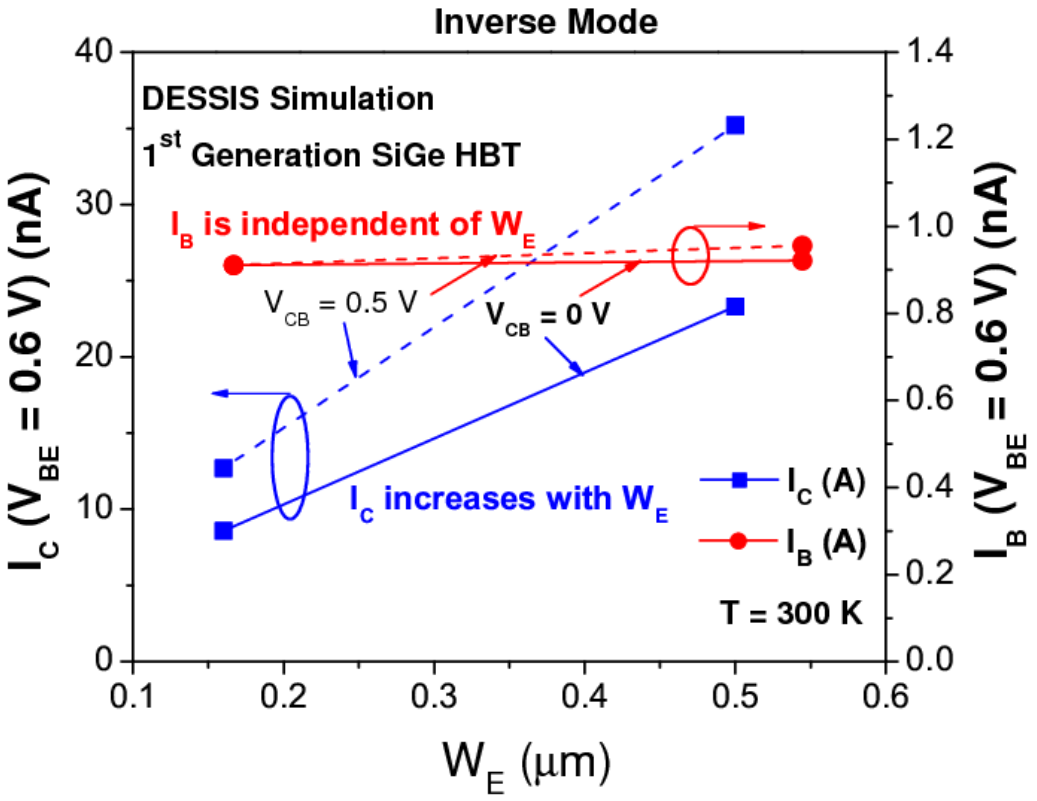


Figure 26. Simulated inverse mode collector and base currents for the nominal device and a laterally scaled version of the first-generation SiGe HBT.

To further verify this, the gain of a minimum geometry device was compared with a wider emitter stripe device, for the second-generation technology. As can be clearly seen in

Figure 27, the current gain improves dramatically for the wider emitter device due to the increase in collector current, while the base current remains fixed by the STI-SIC distance (and therefore does not scale with W_E). In addition, the current gain does not change with the emitter length, since changing the length of the devices scales both the emitter and the base currents, leading to a constant gain. This behavior with the emitter width scaling is consistent across technology generations. In addition, shown in Figure 26, is the behavior of the inverse mode collector and base currents with varying V_{CB}. The base currents remain roughly constant with V_{CB}, as is to be expected for these short base width devices, while the I_{CREV} increase dramatically with V_{CB} due to the germanium grading in the base, as described in [36].

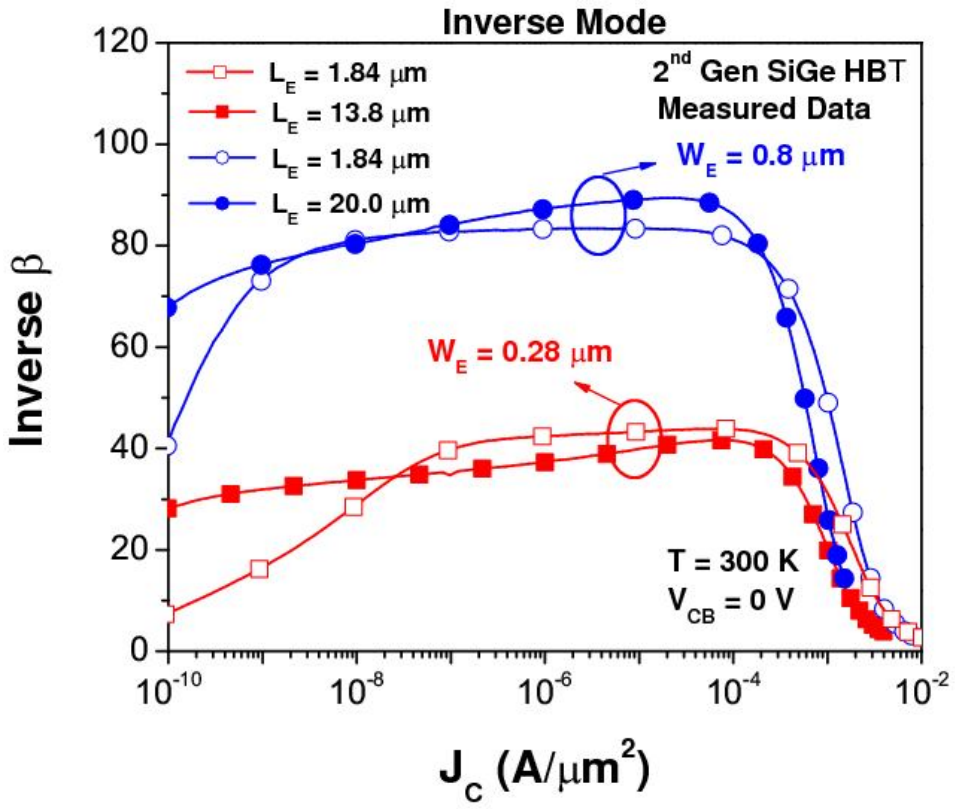


Figure 27. Inverse mode current gain for a second-generation SiGe HBT with different geometries.

The dependence of the inverse mode gain on the emitter width is interesting, since it allows for a new paradigm in inverse-mode device optimization by lateral design changes. In power amplifier applications, for example, wider emitter devices are sometimes preferred for improving output current drive capability and hence power density [39]. Such a device topology would automatically lead to an improved inverse mode performance, and will be important to model accurately, particularly if switching occurs into the saturation regime. At present, many design kits do not properly account for such variations.

To verify the dependence of I_{BREV} on the STI-SIC spacing, we measured devices with varying STI-EN distances (refer to Figure 18) - which effectively varies the STI-SIC spacing. As expected, the base current increases with the STI-EN spacing (Figure 28). Simulation results (not shown here) confirm this behavior. As mentioned previously, the STI-SIC spacing for the second-generation SiGe HBTs is larger than the distance for the first-generation SiGe HBT, contributing to the apparent increase in its J_{BREV}.

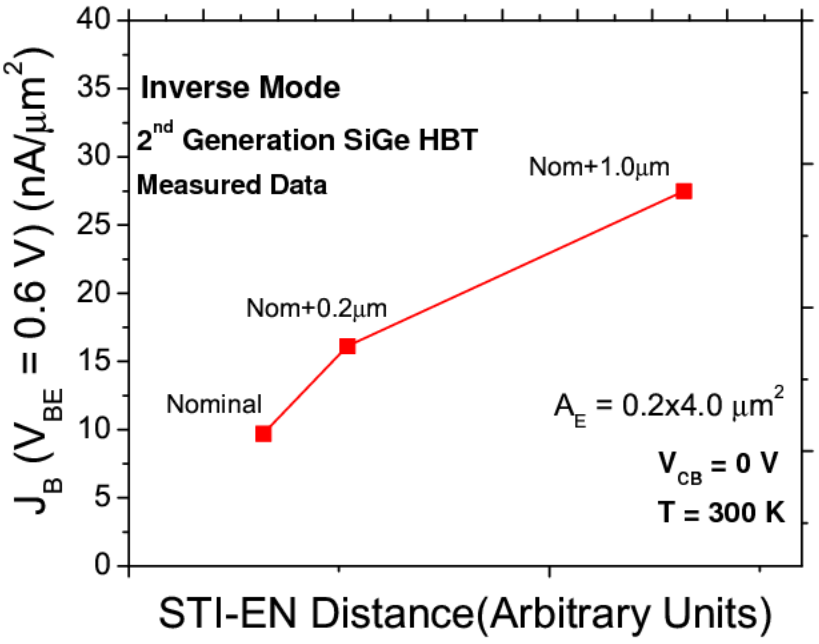


Figure 28. 2nd inverse mode base current densities at V_{BE} = 0.6 V with varying STI-EN spacing.

In the devices examined in this work, J_{CREV} increases from the first- to the second-generation device, since the forward (I_{CF}) and inverse mode collector currents (I_{CREV}) overlay for all technology generations [36] and I_{CF} increases significantly for the second-generation device, as discussed above. The increase in I_{CREV} for these second-generation devices compensates for the increased base current in the inverse mode, leading to an increase in inverse mode current gain.

A comparison of J_{BREV} of the second- and third-generation devices reveals a significantly smaller J_{BREV} for the third-generation devices (Figure 23). Although comparing inverse mode current densities between devices of varying geometry is potentially misleading, as explained above, the emitter width of these two devices are comparable, and so is their STI to SIC spacing. Considering the similarities, we believe that the observed differences in the base currents are due to the structural differences in the extrinsic base. That is, the third-generation device has a raised extrinsic base structure, which removes the highly doped p^+ region away from the vicinity of the physical collector region, and therefore could be contributing to decreased recombination currents due to injection of electrons into the extrinsic base. To verify this hypothesis, the second-generation device was simulated by changing its extrinsic base structure to a raised extrinsic base, and a significant reduction in J_{BREV} was in fact observed (Figure 29).

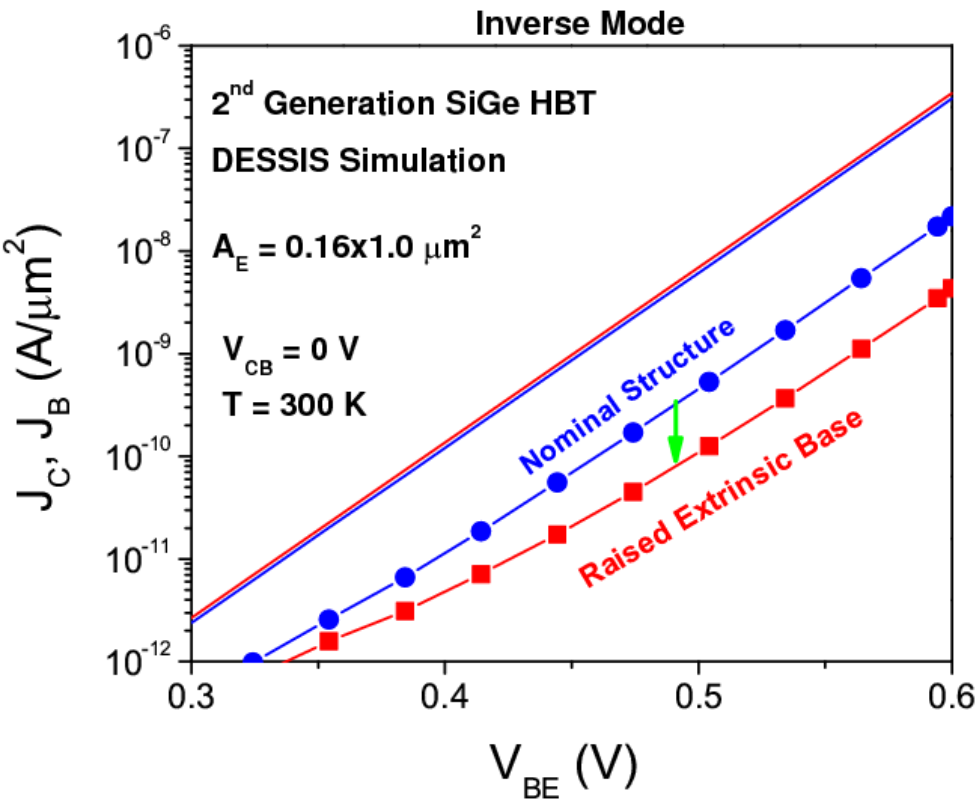


Figure 29. Simulated inverse mode Gummel with different extrinsic base structures.

The influence of the raised extrinsic base structure on the base current was further confirmed by a comparing the third- and fourth-generation devices operating in inverse mode (Figure 24). These devices have identical lateral structure (only vertical scaling was employed for performance enhancement) and therefore an identical J_{BREV} is expected. As can be seen from Figure 4d, the inverse mode base currents indeed overlay over several orders of magnitude, while the collector current increases for the fourth-generation device. The increase in I_{CREV} is again a consequence of the reduced base Gummel number and is reflected in the forward mode collector current as well (refer to Figure 19).

2.3.2 Current Gain Roll-Off

At low to medium injection levels, the current gain behavior of the forward and inverse mode of operation is strikingly different (Figure 30). In the forward mode, the inverse Early effect is enhanced by the germanium grading, leading to a gradual reduction in the forward mode β with increasing J_{CF}, while the inverse mode gain remains roughly constant with J_{CREV}. The inverse mode β remains roughly constant due to the germanium grading effect which leads to an ideal collector current.. The ideal inverse mode collector current, when combined with an ideal base current due to relatively low doping in the electrical EB junction, leads to the constant gain behavior of inverse mode.

At high injection, the current gain rolls off for both the forward and inverse mode of operation. The current gain roll-off mechanism in BJTs operating in the forward mode is well understood to be due to high injection effects in the physical collector (i.e., Kirk effect). In SiGe HBTs, the roll off is further accentuated by heterojunction barrier effects, leading to a sharp roll-off in gain once engaged. While operating in the inverse mode, however, the electrical collector is very heavily doped and therefore one would expect the high injection effects in the electrical collector to be significantly delayed in current density. Contrary to this naïve expectation, however, the current gain for the inverse mode actually rolls off at a *lower* current density compared to the forward mode.

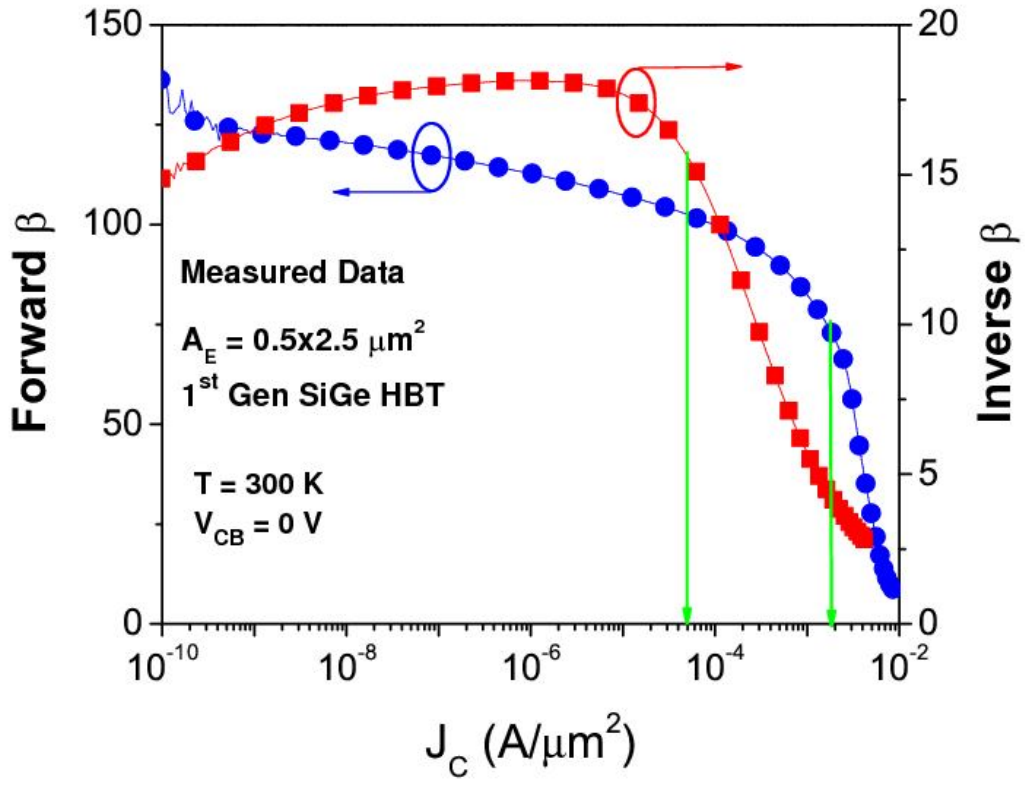


Figure 30. Inverse and forward mode current gain for a first-generation SiGe HBT as a function of J_C.

This difference in gain roll-off behavior was also observed for symmetrically doped devices (in [34]) and it was speculated to be due to the formation of a heterojunction barrier effect in the electrical EB junction. In the present work, we have examined the gain roll-off behavior of a first-generation silicon BJT of identical layout and doping (i.e., it is identical to the SiGe HBT except for the absence of germanium), and which shows the identical roll-off behavior as for the SiGe HBT, clearly disproving the speculation that the observed roll-off is due to the influence of Ge-induced heterojunction barrier effects.

The simulated electron, hole and donor concentrations for a third-generation SiGe HBT operating in the inverse mode, as a function of V_{BE}, are shown in Figure 31, 32. At medium

injection (Figure 31), the electron profile follows the doping concentration in the electrical emitter, as expected. At high injection (V_{BE} = 1.0 V), however, the electron concentration exceeds the doping concentration in the electrical emitter, leading to holes being injected into the emitter, as required to maintain charge neutrality (Figure 32). This effect directly leads to the roll-off in current gain, and is not heterojunction induced. The mechanism of roll-off in gain between the forward and inverse mode of operation is, therefore, identical; namely, high injection effects in the physical collector. In addition, at the highest current densities (~ 5 mA/μm^2), self-heating clearly also influences the roll-off, with an estimated increase of about 20 K over the ambient temperature of 300 K.

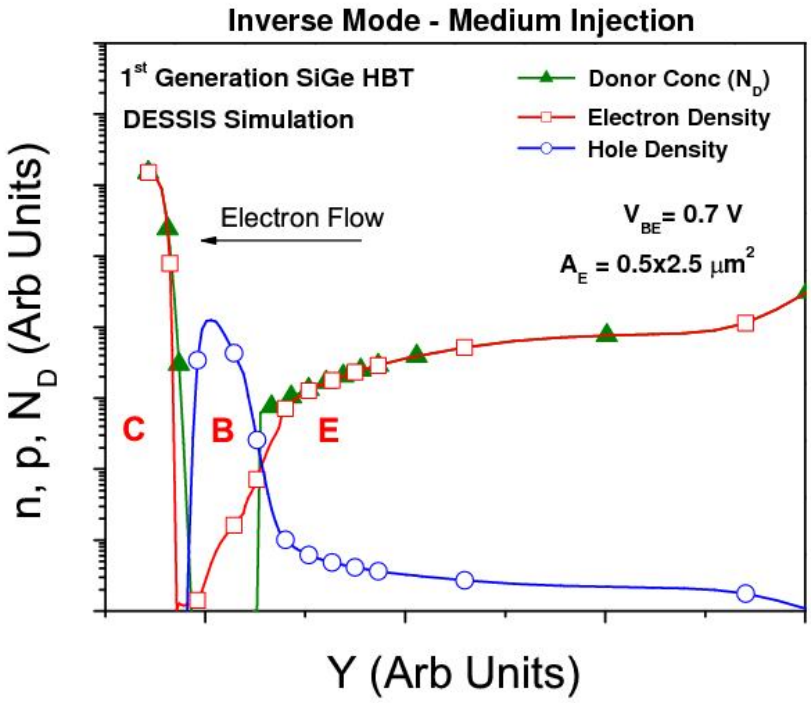


Figure 31. Simulated electron and hole profiles for inverse mode operation in a first-generation SiGe HBT for medium injection

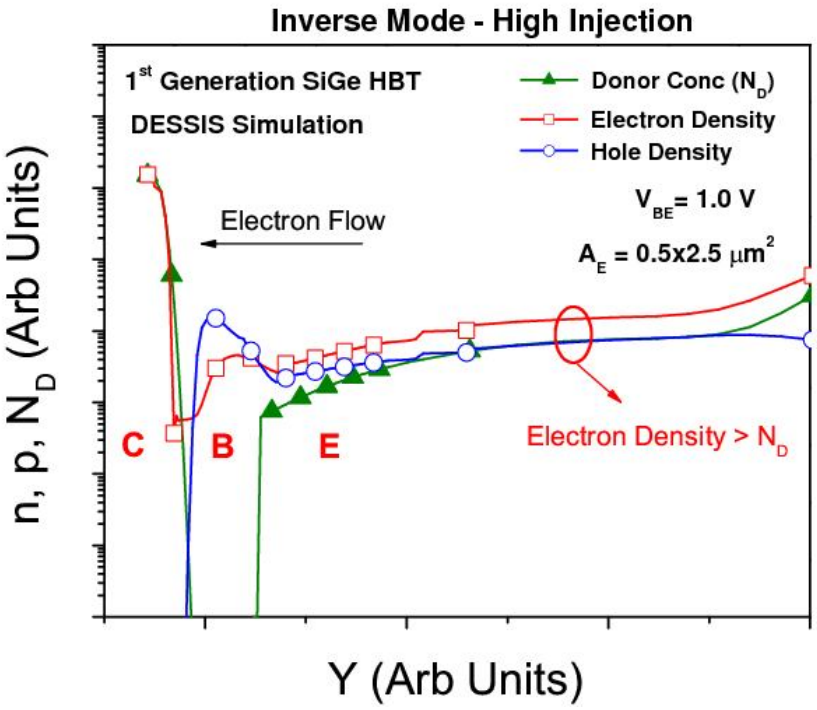


Figure 32. Simulated electron and hole profiles for inverse mode operation in a first-generation SiGe HBT for high injection.

Although the high injection roll-off effect occurs in the physical collector for both the forward and inverse mode, the required current density at the point of high injection is smaller for the inverse mode due to the smaller velocity of electrons in the forward-biased physical collector when compared to the depleted collector in the forward mode (i.e., J= qnv). The physical collector doping profile thus influences the gain roll-off and the emitter resistance in inverse mode, thereby limiting the drive currents in the inverse mode.

2.3.3 *ac* Performance

The S-parameters were measured to 40 GHz on specially designed test structures (i.e., in common- collector configuration) and subsequently de-embedded using standard techniques. The extracted h_{21} was then used to extract the f_T. The f_T of the third- and fourth-generation devices as

a function of collector current is shown in Figure 33. The peak f_T increases from 10.5 GHz for the third-generation device (200 GHz in forward mode) to a value of 22 GHz for the fourth-generation device (300 GHz in forward mode) at a V_{CB} of 0 V. The inverse mode performance improves to about 12 GHz peak f_T for the third-generation device at a V_{CB} of 0.5 V and 25 GHz for the fourth-generation device at a V_{CB} of 0.25 V. The f_T values (and current gain) are large enough from a circuit perspective to be potentially useful in designing novel circuits where raw speed is not the main driving force (e.g., analog), and this opportunity is currently being explored.

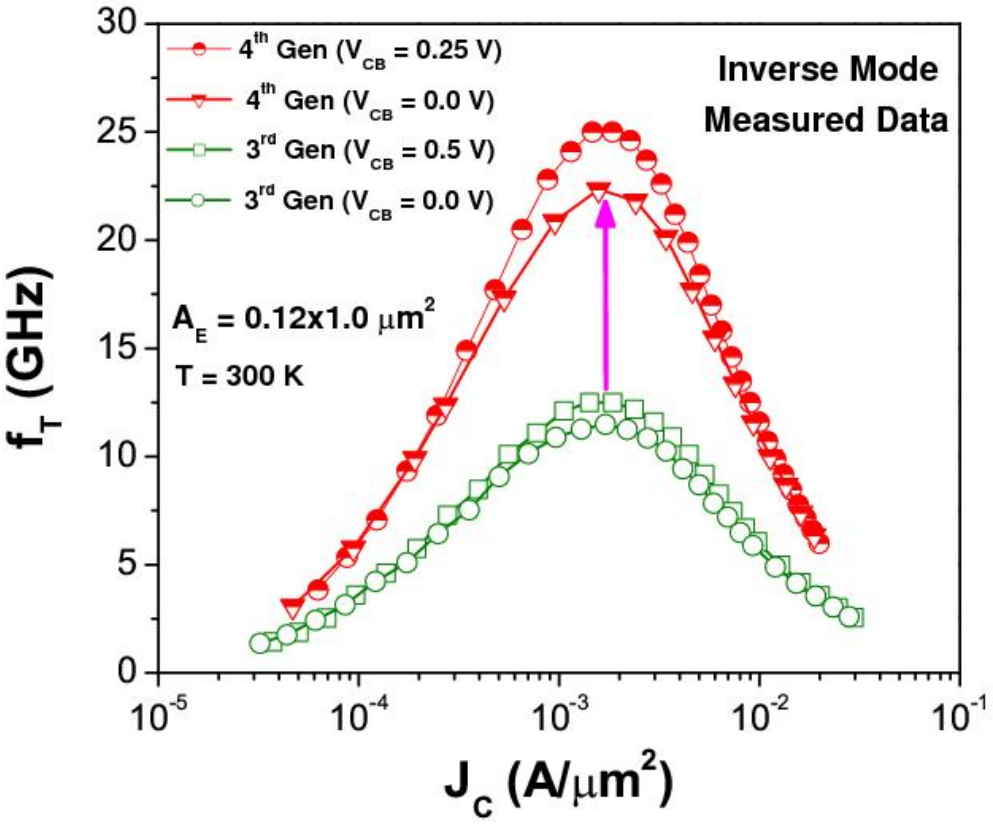


Figure 33. Cutoff frequency as a function of collector current for third- and fourth-generation SiGe HBTs.

To understand the inverse mode f_T performance, we performed calibrated 2D transit time simulations for the third-generation device operating in the inverse mode in order to identify the limiting transit time component(s). This would help us predict future inverse mode *ac* performance of more aggressive SiGe technology nodes, based on reasonable assumptions on doping and physical scaling trends. The transit time was calculated along current contours, and integrated to get the total transit time contributions from the emitter to the collector contact. The 2D transit time extraction methodology is explained in more detail in [40, 2]. The calculated accumulated transit time at J_C (peak f_T) for one dominant sample current contour is shown in Figure 34. The decrease in the accumulated transit time near the physical emitter-base junction could be due to a change in the electron density at that point. As is clearly seen in the figure, the inverse mode transit time is limited by the base transit time near peak f_T. This is due to the negative electric field in the base (for inverse mode operation) due to germanium grading.

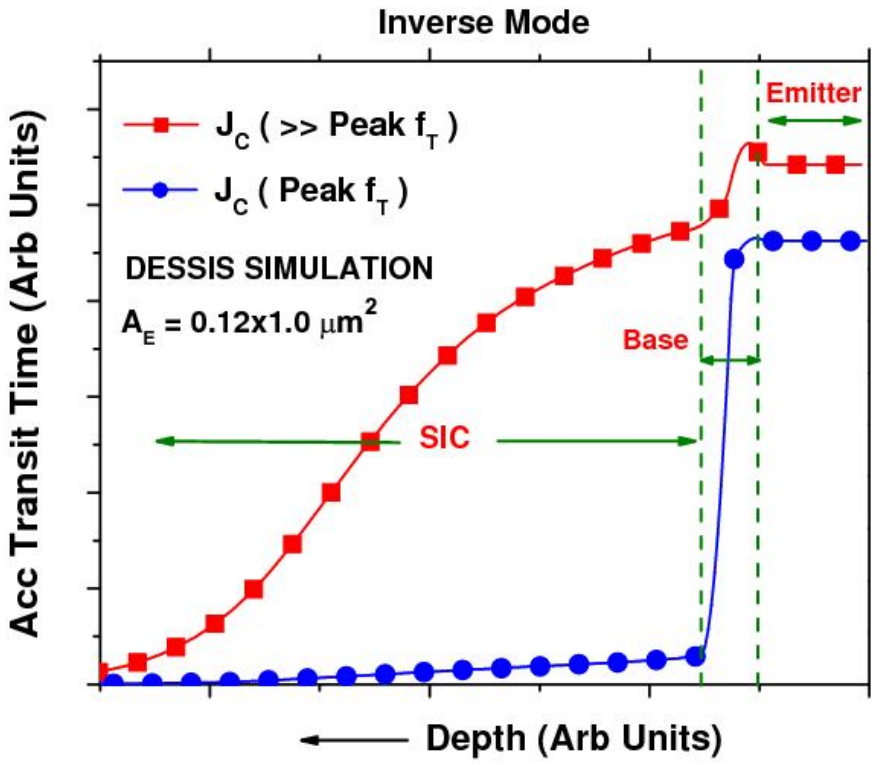


Figure 34. Simulated 2D accumulated transit time for inverse mode operation of a third-generation SiGe HBT biased at peak f_T and at much greater than peak f_T.

The transit time simulation does not differentiate between regions within the base and it is possible that the transit time is dominated by extrinsic base charge storage. This would be revisited in the examination of cryogenic inverse mode performance of SiGe HBTs.

The depletion and diffusion capacitance terms can be extracted from the f_T on J_C characteristics [2]. The extracted capacitance and transit time components are shown in Figure 35. The total transit time at peak f_T for the third and fourth generation devices are calculated as $1/(2\pi f_T)$ to be 15.16 and 6.9 ps, respectively. As is clearly seen from Figure 35, the sum of the emitter and base transit times (τ_{REV}) dominate the total transit time. With a V_{CB} of 0.5V, the third generation devices show a decrease in τ_{REV} from 11.04 ps to 8.76 ps, a 20 % reduction, which translates to the ~ 14% improvement in peak f_T. This reduction is due to the decrease of the

retarding field in the base due to germanium grading and due to the improved gain due to the large inverse mode output conductance [36]. The τ_{REV} of the fourth generation devices similarly improves by ~17 % for a V_{CB} of 0.25 V.

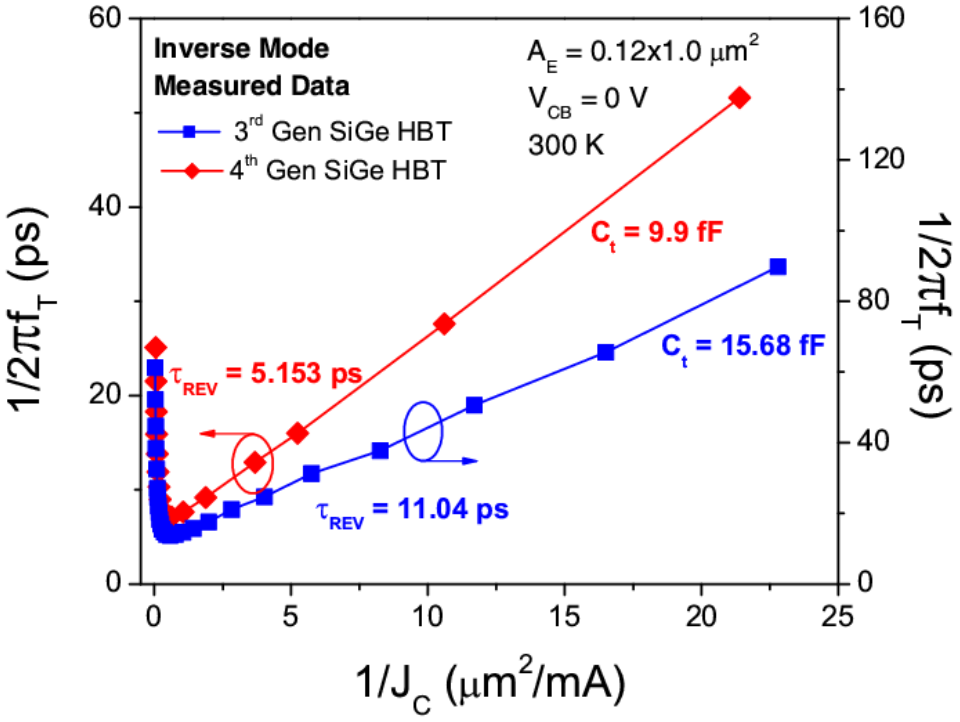


Figure 35. Transit time and depletion capacitance contributions to the inverse mode f_T for the second and third generation SiGe HBTs.

The f_T roll-off in the forward mode is known to be due to the Kirk effect and barrier effect, which rapidly increases the base transit time once engaged. The absence of Kirk effect in the inverse mode of operation (due to the heavy electrical collector doping) implies that the roll-off in f_T at high currents cannot be due to an increase in base transit time. A simulation of the inverse transit time at a point beyond J_C at peak f_T clearly shows that the increase in transit time through the SIC region due to the roll-off in current gain is the dominant performance limiting mechanism (Figure 34).

Chapter 3

Optimization of Inverse Mode Performance of SiGe HBTs

In the previous chapter, the physics of inverse mode operation was examined and the transit time limitations on inverse mode performance were identified. While inverse mode performance improves significantly with generational scaling, there is a definite need for further improvement in inverse mode performance to enable its widespread application in high-speed digital and RF circuits. In this chapter, optimized device structures are described which improve inverse mode performance of SiGe HBTs dramatically. The improvement in performance is illustrated by a combination of TCAD and measured data. These results were published earlier in [47, 48, 49]

3.1 Layout Optimization of SiGe HBTs for Inverse Mode Performance

Optimized collector-up SiGe HBTs have been previously reported [34-35]. Here we describe, for the first time, new ways to further optimize inverse-mode performance of SiGe HBTs, utilizing only minor layout modifications. These changes can in principle be implemented in any SiGe technology platform.

The examination of the physics of inverse mode operation with scaling gives valuable insights into the transit time limiting mechanisms in inverse mode and suggest ways to improve performance. The following sets of optimizations (that are fully compatible with existing fabrication techniques) suggest themselves:

1. The STI-SIC distance needs to be minimized for improving the current gain and reducing any external capacitances. Also, the removal of the extrinsic physical collector will lead to a reduction in the injection of carriers into the extrinsic region which could lead to further improvement in performance.
2. For inverse mode performance, a raised extrinsic base architecture is more optimal than a self-aligned extrinsic base.
3. A larger emitter width would lead to better current gain and would reduce the emitter charge storage in inverse mode.
4. A higher collector doping (N_c) would increase the current at which the gain rolls-off leading to reduced capacitive delays.

TCAD simulations (Figure 36) predict an improvement in the inverse mode f_T of a third generation SiGe HBT with emitter width. The f_{max} of the transistor however degrades with larger emitter width.

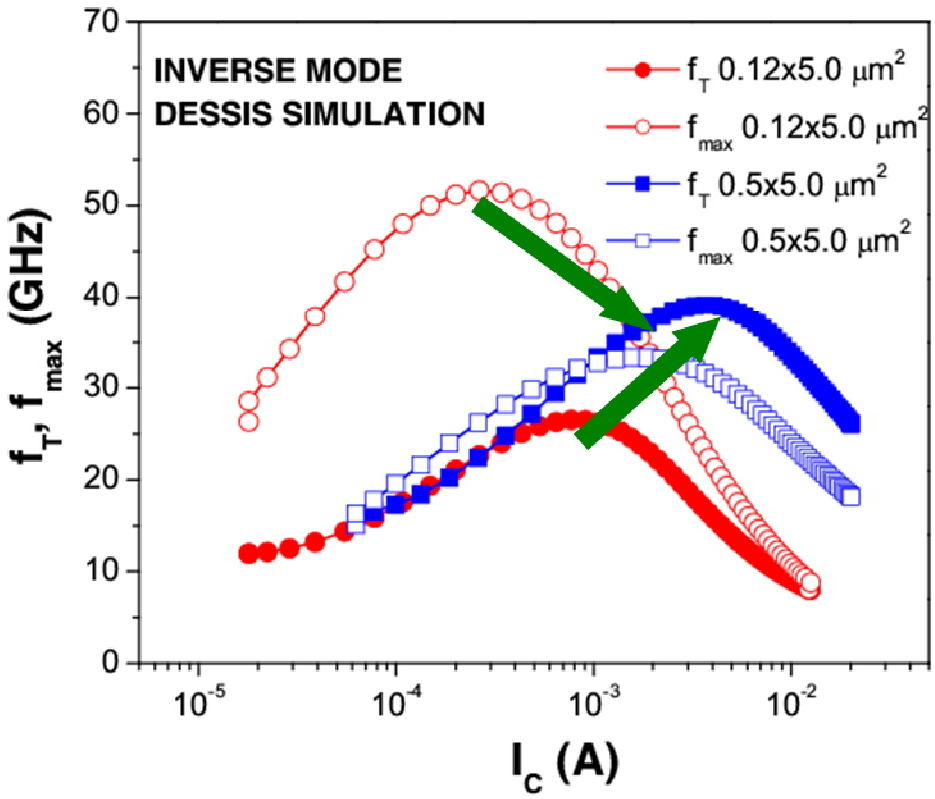


Figure 36. TCAD simulations of inverse mode operation of SiGe HBTs

Based on the above, test structures were laid out in a third generation high performance (high N_C) SiGe HBT, which employs a raised extrinsic base structure. Devices with different emitter widths and varying STI-SIC spacing were examined for DC and AC performance. Shown in Figure 37 are the Gummel characteristics of the laid out structures. As can be seen from the figure, for devices of increasing width, the collector current scales up with geometry while the base current remains fixed. This leads to an improvement in current gain as seen in Figure 38.

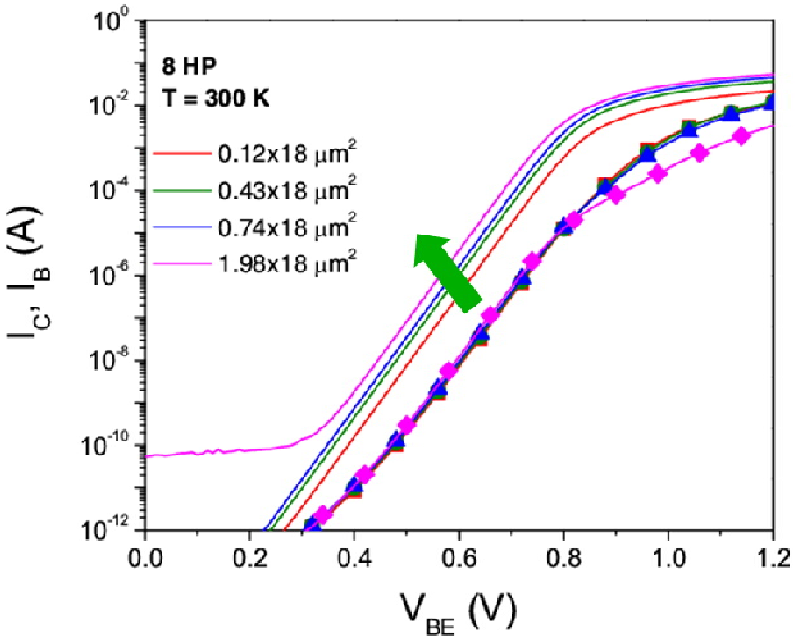


Figure 37. Inverse Gummel characteristics of third generation SiGe HBTs of different widths

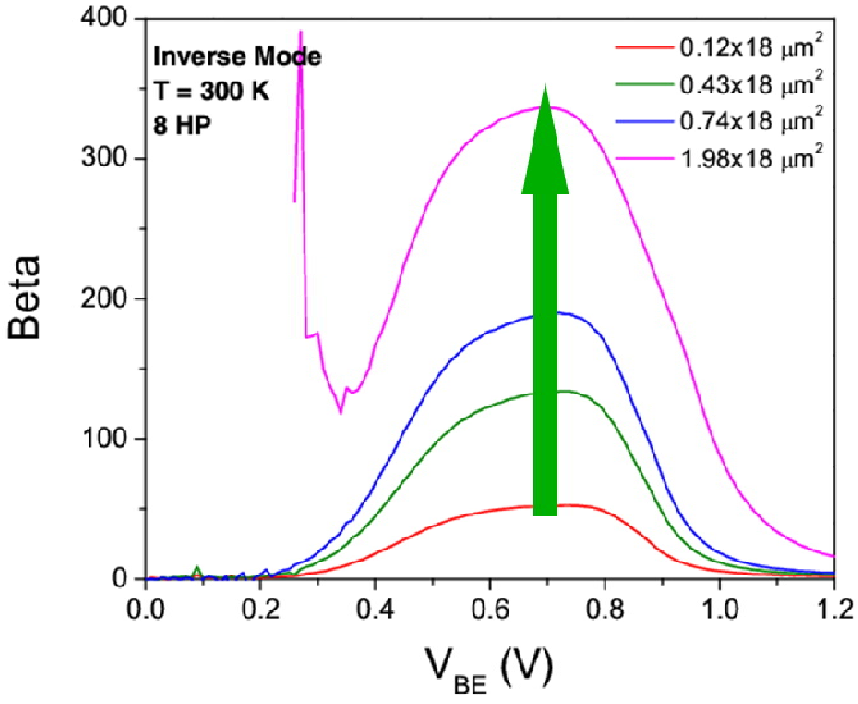


Figure 38. Inverse mode current gain of third generation SiGe HBTs of different widths

The improvement in DC gain also translates into a significant improvement in dynamic performance. The improvement in DC current gain (from a peak of 80 to 150) with device width (from 0.12 to 0.5 μm), translates into a measured 100% improvement in the peak f_T from 7.5 GHz to 15 GHz, as seen in Figure 39.. A further increase in the device width from 0.50 μm to 0.80 μm does not improve the f_T significantly, in spite of further improvement in β, suggesting that base transit time now dominates the total transit delay. The performance can still be improved, however, by decreasing the width of the extrinsic collector region by drawing the shallow trench isolation oxide (STI) closer to the intrinsic collector (in this case 0.19 μm closer than for the nominal design) , which reduces the charge injected into the extrinsic base from the extrinsic collector. This second optimization step results in a doubling in peak f_T from 15 GHz to 31 GHz. The extracted transit times (generated from a plot of $1/f_T$ versus $1/I_C$ – Figure 41) decrease from 20 ps for the nominal device, to 9 ps for the wider device, to 5 ps for the final optimized device. This improvement in f_T through only layout modifications is also predicted in calibrated TCAD simulations. The improvement in f_T by purely increasing the width of the device, however, comes at the cost of a 43% reduction in peak f_{max} (from 28 GHz to 23 GHz to 16 GHz – Figure 40) due to increased base resistance and collector-base capacitance. However, the f_{max} can be recovered in the fully optimized structures, with f_{max} improving to 32 GHz for a 0.2 μm wide device. We are currently examining the leverage of the improved f_T in the optimized structures in digital bipolar gates [41]. Also shown in the plot are results after 600 krad of X-ray irradiation. No significant change in f_T or f_{max} is observed, demonstrating the total dose hardness of inverse mode SiGe HBTs. The total dose tolerance of inverse mode SiGe HBTs after proton and gamma radiation has been reported in [42, 43], where less than 15 % degradation in current gain at peak f_T bias was observed after 1 Mrad irradiation.

An additional concern associated with the use of inverse-mode operated SiGe HBTs is its operating voltage limitation due to the high electric fields in the physical emitter-base junction. The inverse-mode BV_{CEO} for a nominal device (A_E = 0.12x6.0 μm^2) was extracted from forced-V_{BE} output characteristics and is found to be 1.4 V, which is adequate for high-speed CML/ECL circuits, where the typical worst case collector-emitter voltage does not exceed 0.8 V. This reasonably high BV_{CEO} can be attributed to the rather low current gain in inverse mode (~80) and has been observed in other technologies as well [44]. The optimized inverse-mode devices (A_E = 0.8x6.0 μm^2), however, are designed for higher β (~650) and consequently show a reduced, albeit still acceptable, BV_{CEO} of 1.2 V. The breakdown voltage, however, can be improved by using a narrower device since a gain of ~150 is found to be sufficient to reduce the emitter transit time to reasonable levels. The reliability of nominal width devices was also characterized with the conventional (reverse-biased physical emitter-base junction) open-collector (OC) stress (V_{EB} = 3.0 V) and forward-biased collector (FC) stress (J_C = 1.3 mA/μm^2 to 7.8 mA/μm^2, with V_{EB} = 2.0 V), and the stress damage was limited to less than 5% degradation in gain at the peak f_T bias point (V_{BE} = 0.8 V) for 1,000 seconds of stress, suggesting that the reliability of the inverse-mode devices should be adequate for robust circuits.

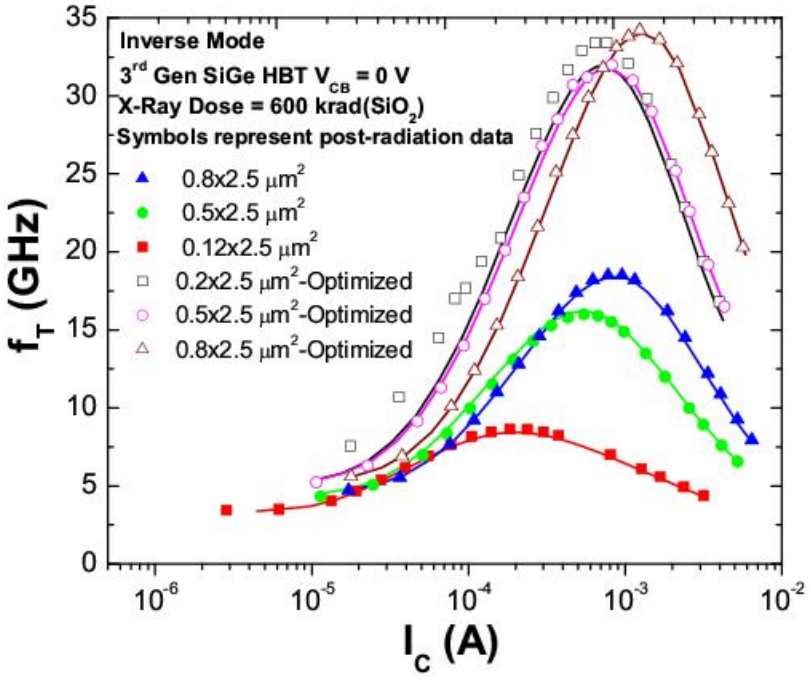


Figure 39. Inverse mode f_T as a function of inverse mode collector current for optimized test structures

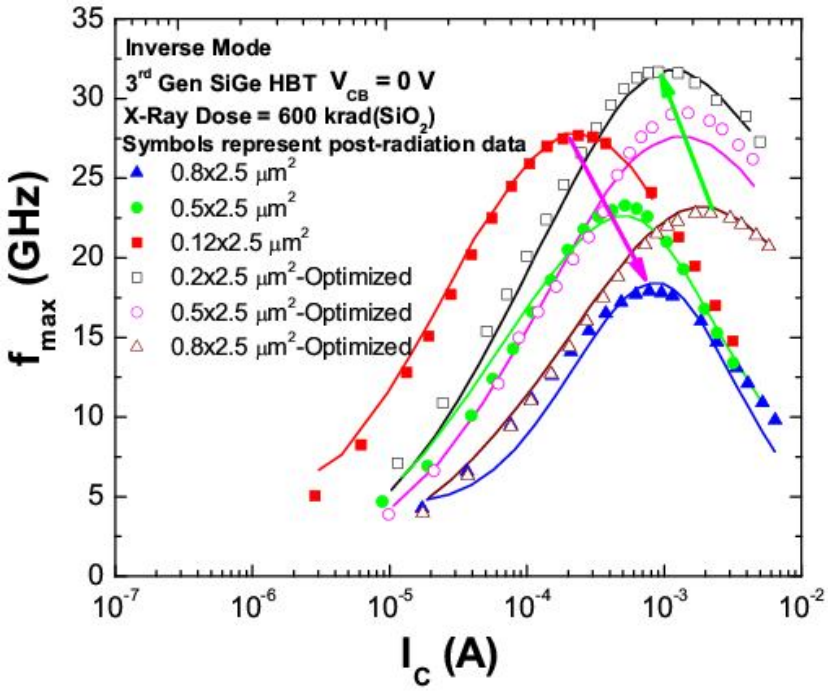


Figure 40. Inverse mode f_{max} as a function of inverse mode collector current for optimized test structures

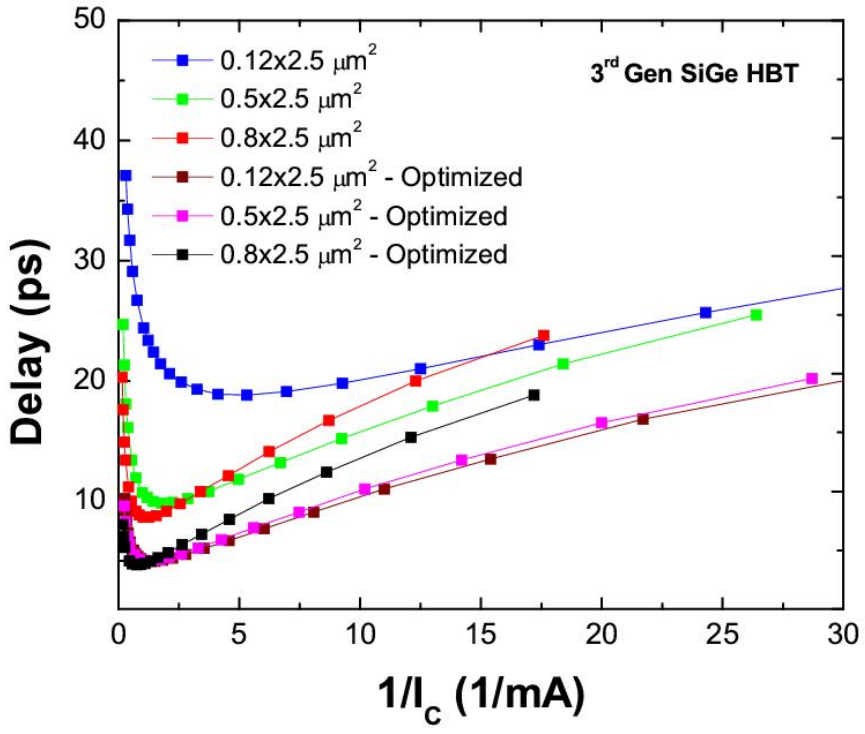


Figure 41. Transit time extraction for inverse mode transistors

3.2 Inverse Cascode Structure

While the inverse mode performance of SiGe HBTs is improved significantly using layout modifications as demonstrated in the previous section, for very high-speed circuits, the performance of optimized inverse mode SiGe HBTs might be inadequate. One could, however, improve the inverse mode performance of SiGe HBTs further by combining an inverse mode device with a forward mode device in a cascode configuration as shown in Figure 42. The "inverse cascode" SiGe HBT combines the SEU hardness of an inverse mode device with the high speed performance of a forward mode device.

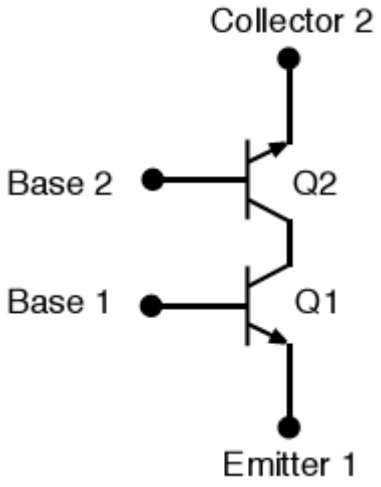


Figure 42. Inverse cascode device schematic

The SEU hardness of the inverse cascode device arises out of the fact that a current pulse injected at the collector node of the forward mode transistor is split between the forward mode and inverse mode transistors. Also, the common terminal between the forward and inverse mode transistor could accommodate a capacitor that acts as a shunt path for the SEU transient currents.

The forward mode transistor provides most of the small signal current gain of the cascode device while the inverse mode transistor is biased in a common base configuration with no current gain. The f_T of discrete cascode devices as function of collector current, with the top device operating in forward or inverse mode, is shown in Figure 43. The cascode structure with both the top and bottom device operating in forward mode provides the maximum gain with a peak f_T of 190 GHz, which is comparable to the performance of a forward mode SiGe HBT. As expected, the performance of the inverse mode SiGe HBT is dramatically improved when cascoded with a forward mode device. The peak f_T for the inverse mode cascoded structure employing an un-optimized nominal width device improves from a nominal value of 8 GHz to

80 GHz. By employing an inverse mode device with a larger emitter width of 0.5 um, the peak f_T improves to ~125 GHz. The improvement in performance for the larger device arises out of the difference in forward and inverse mode peak f_T current densities. The current density at peak f_T for an inverse mode device is about an order of magnitude smaller than the current density at peak f_T for a forward mode device as seen in figure 44. By employing a wider inverse mode device in the cascode eonfiguration, both the bottom and top HBTs are operated at near the peak f_T current density which leads to this improvement in performance. This is confirmed by the fact that a cascode device with a larger emitter length as compared to the forward mode device also shows a similar improvement in peak f_T, in spite of the fact that the inverse mode performance of devices of different lengths is comparable.

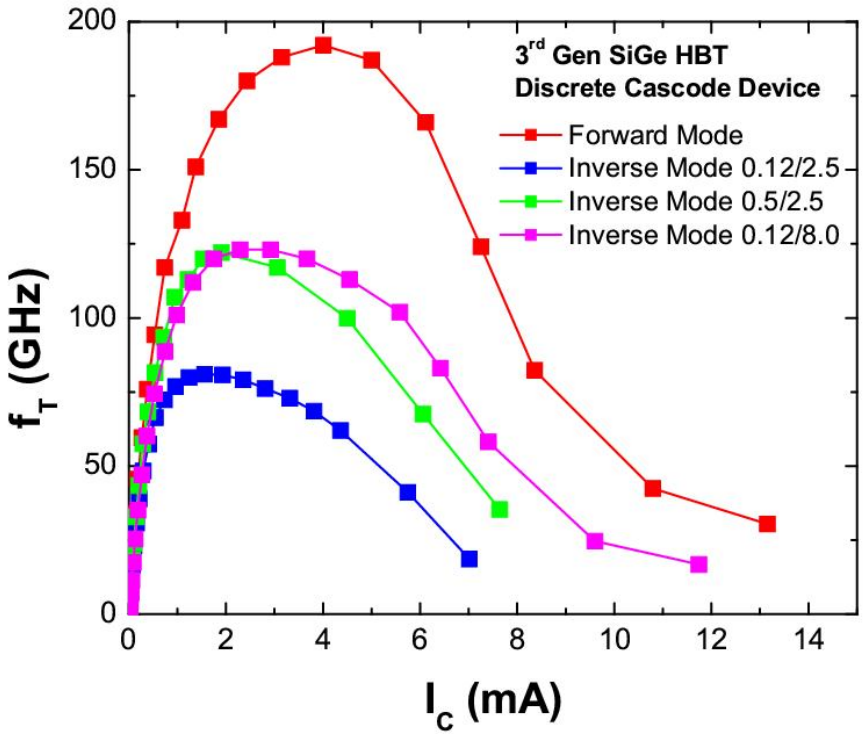


Figure 43. f_T as a function of collector current for different discrete cascode devices

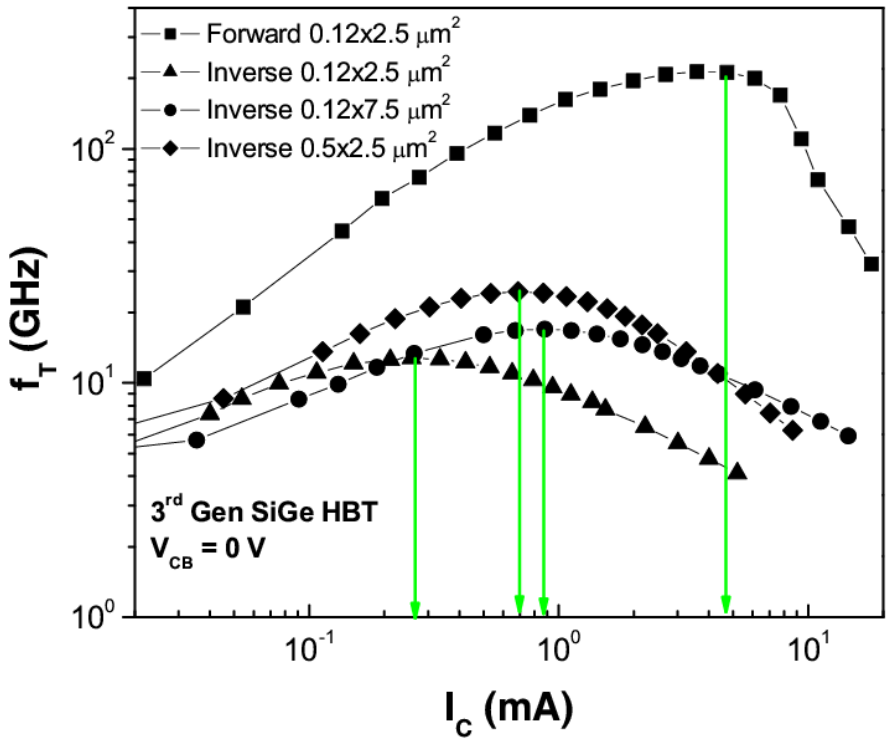


Figure 44. f_T as a function of collector currents for forward and inverse mode SiGe HBTs

While the cascode architecture offers many significant advantages, it has two major drawbacks. The use of two transistors imposes constraints on the minimum rail voltage that can be used and two discrete devices occupy twice the device area as compared to a single discrete device. The area penalty associated with the cascode structure can however be mitigated by integrating the common base inverse mode device with the forward mode common emitter transistor through the common subcollector node. A schematic illustration of the same is shown in Figure 45. By using an inverse mode transistor as the common base device, the two transistors can be integrated in one device without any area penalty. The top view of the laid out device structure is shown in Figure 46. For comparison a single SiGe HBT in a CBEBC configuration is juxtaposed and one can observe that the active device areas are identical for the cascode device

and the single transistor. For this nominal device configuration, no design rules are violated and the yield of the device can therefore be expected to be similar to the nominal discrete HBT.

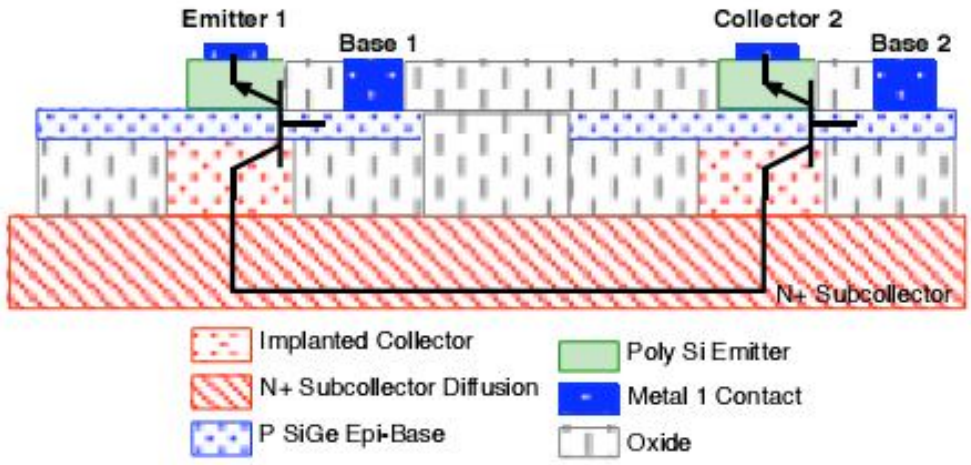


Figure 45. Structure of an integrated inverse cascode device

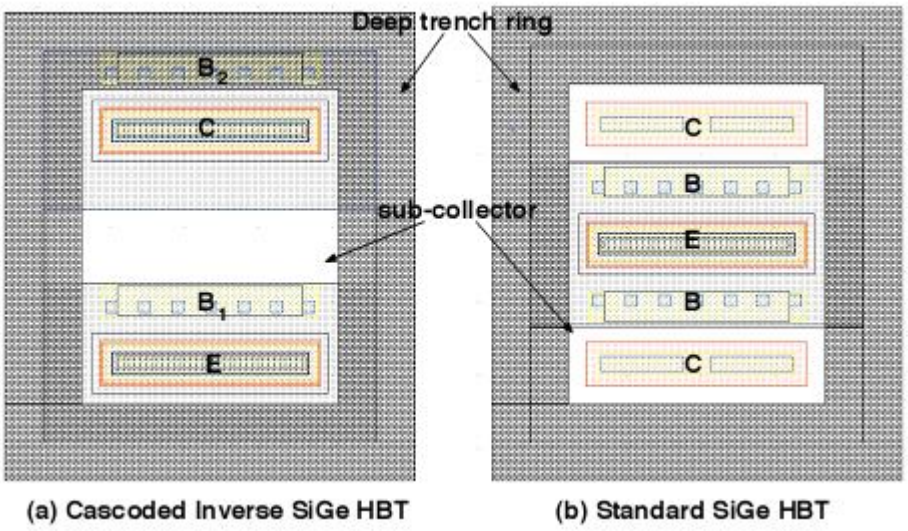


Figure 46. Top view of an inverse cascode SiGe HBT and discrete CBEBC SiGe HBT

The integrated inverse cascode device shows comparable performance to the discrete cascode devices with a peak f_T of 120 GHz. The f_T of the integrated inverse cascode device as a

function of collector current is shown in Figure 47. The inverse mode transistor here has a width of 0.5 μm to optimize the cascode device performance. The nominal inverse mode transistor in the cascode configuration has a peak f_T of 70 GHz. For the integrated device, the device length is fixed by the forward mode transistor but the device width of the inverse mode transistor can be varied independent of the forward mode transistor. This dictated the use of a wider inverse mode transistor to optimize the cascode device performance. Also shown in the figure is the TID tolerance of the integrated inverse cascode device. The device characteristics show negligible change after 1 Mrad of X-ray radiation exposure. This combination of TID tolerance, excellent device performance and SEU hardness in a commercial off-the-shelf technology with no process modification is clearly good news for extreme environment applications.

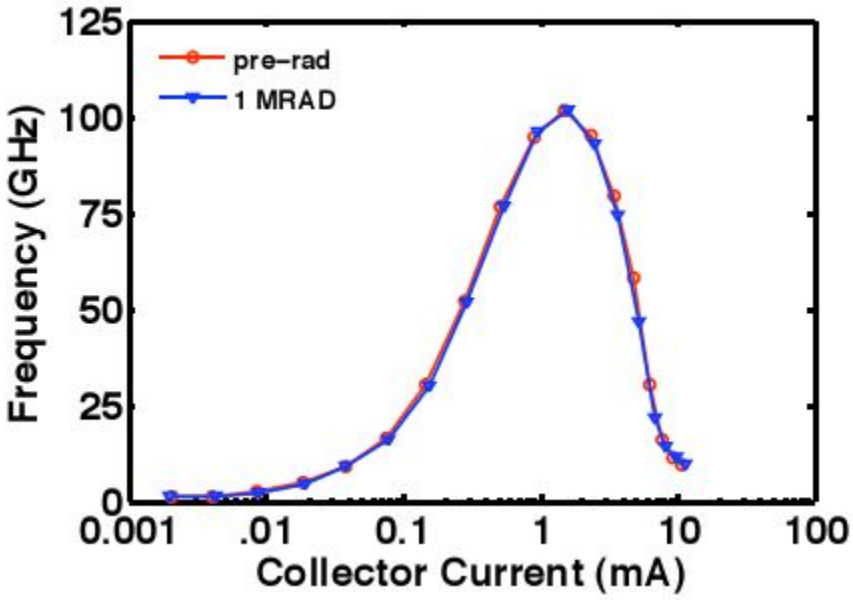


Figure 47. f_T of integrated inverse cascode SiGe HBT as a function of collector current

3.3 TCAD Simulation of Inverse Mode Performance

In the previous sections, the performance of inverse mode transistors were shown to improve significantly by purely layout modifications. While this is clearly good news from a cost perspective, it is also interesting to explore ways to optimize the inverse mode device performance through optimal device profiles. An optimal device structure for inverse mode performance is shown in Figure 48. As discussed previously, the STI of the transistor is drawn close to the SIC to minimize injection of charge carriers into the extrinsic device regions. In addition, the germanium profile of the SiGe HBT is flipped from its nominal value to provide an accelerating field for charge carriers injected into the base from the physical collector. These two modifications alone resulted in device with peak f_T of 170 GHz as shown in Figure 49. It is therefore possible to achieve high levels of performance in inverse mode SiGe HBTs through simple processing optimizations.

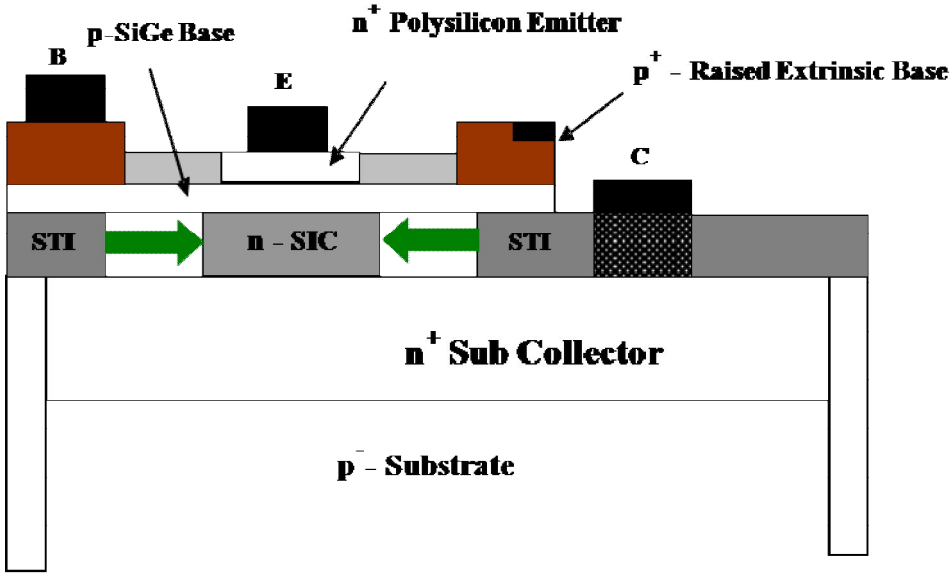


Figure 48. Structural modifications for inverse mode optimization

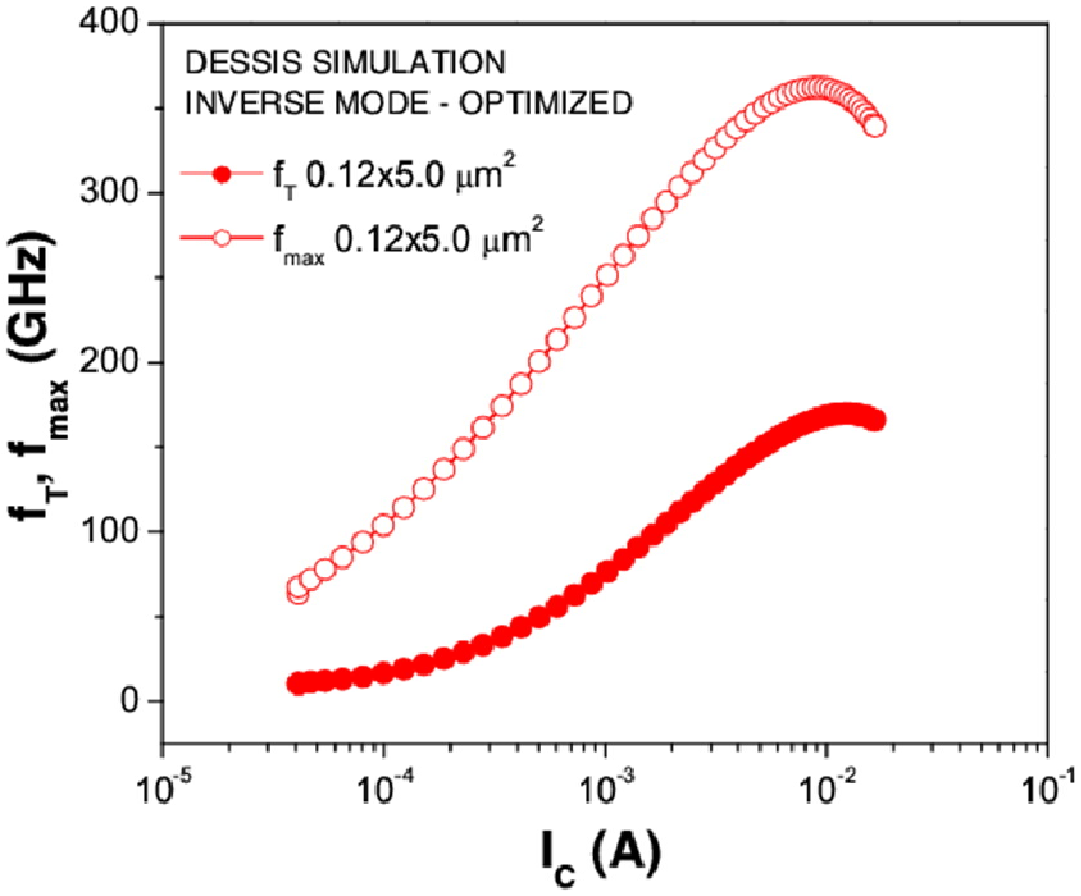


Figure 49. Inverse mode SiGe HBT performance for optimal device profiles

Chapter 4

Cryogenic Operation of Inverse Mode of SiGe HBTs

As discussed in the earlier chapters, the TID tolerance and SEU hardness of inverse mode SiGe HBTs make them potential candidates for extreme environment applications. For application in space, however, in addition to radiation tolerance, devices have to be operable at cryogenic temperatures. In this chapter, the cryogenic performance of inverse mode SiGe HBTs is examined. Since SiGe HBTs are highly influenced by band structure, the effect of germanium in the base of these devices is amplified at lower temperatures. An examination of the performance of SiGe HBTs at reduced temperature, therefore, also provides further insights into the physics of operation at all temperatures and is a useful tool for optimization schemes in both the forward and inverse mode. The results to be discussed here were published earlier in [48].

The forward and inverse collector currents of a first and third generation SiGe HBT is shown in Figure 50 and 51, respectively. The forward and inverse mode collector currents overlay nicely at room temperature (Figure 50, 51), since both the base Gummel number and the effective emitter area are identical for forward and inverse mode operation [36]. At reduced temperatures, however, the inverse mode collector current clearly exceeds the forward mode, with the ratio increasing with cooling (Figure 50, 51). This is due to the difference in forward and inverse mode Early voltages, resulting from the finite Ge grading across the base of the SiGe HBT. The different temperature dependence of the inverse and forward mode Early voltages translates into a difference in the collector current ideality. While the forward mode ideality degrades with cooling, the inverse mode collector current ideality improves with cooling. Note that this

difference is thermally activated and is technology generation dependent and is exaggerated for scaled technologies due to the naturally increased Ge grading across the base (Figure 51).

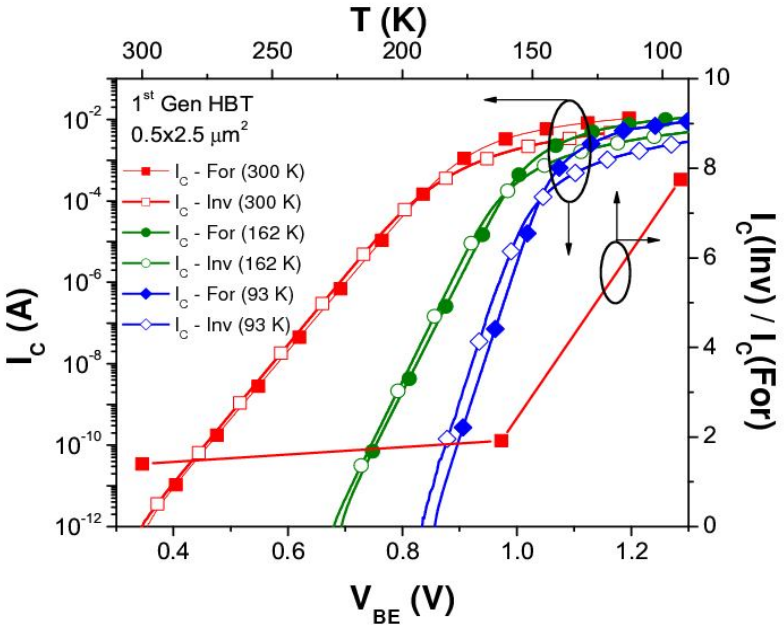


Figure 50. Forward and inverse mode collector currents as a function of temperature. The ratio of the collector currents increases at reduced temperatures.(1st Gen)

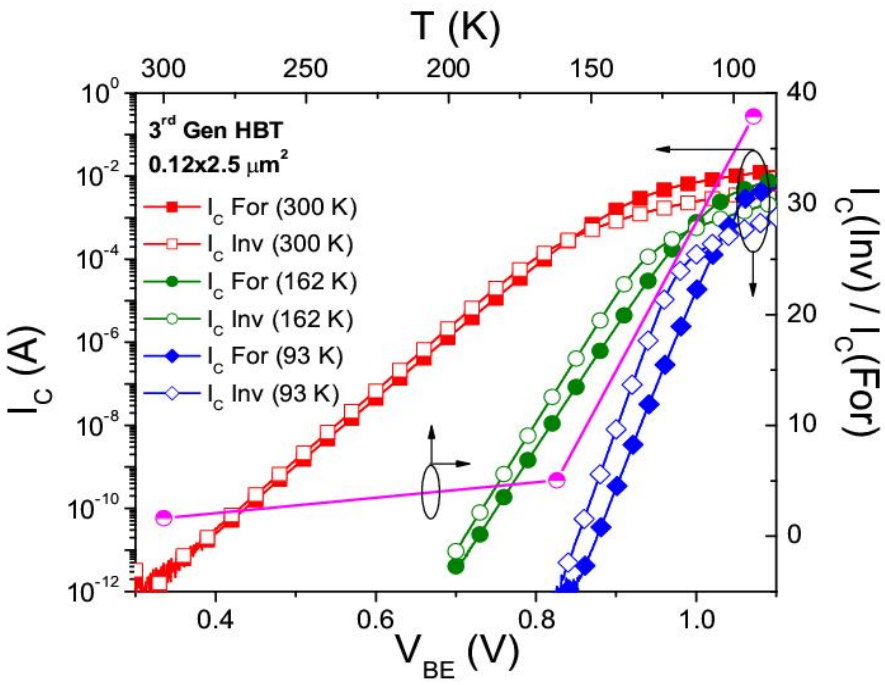


Figure 51 Forward and inverse mode collector currents as a function of temperature. The ratio of the collector currents increases at reduced temperatures (3rd Gen).

Shown in Figure 52 are the inverse mode Gummel characteristics, as a function of temperature, for a third generation SiGe HBT. The corresponding current gain is shown in Figure 53. At low-to-medium injection levels, the current gain of the device in the inverse mode decreases with cooling despite the increased collector currents compared to the forward mode, as explained above. It is to be noted that the forward mode current gain increases significantly at lower temperatures. Clearly, this decrease in gain is driven by an increased base current in inverse mode. In addition, one observes that there is an unexpected **dramatic** current gain improvement at high injection in inverse mode, which is in contrast to the usual thermally-activated sharp roll-off in current gain at reduced temperatures in the forward mode.

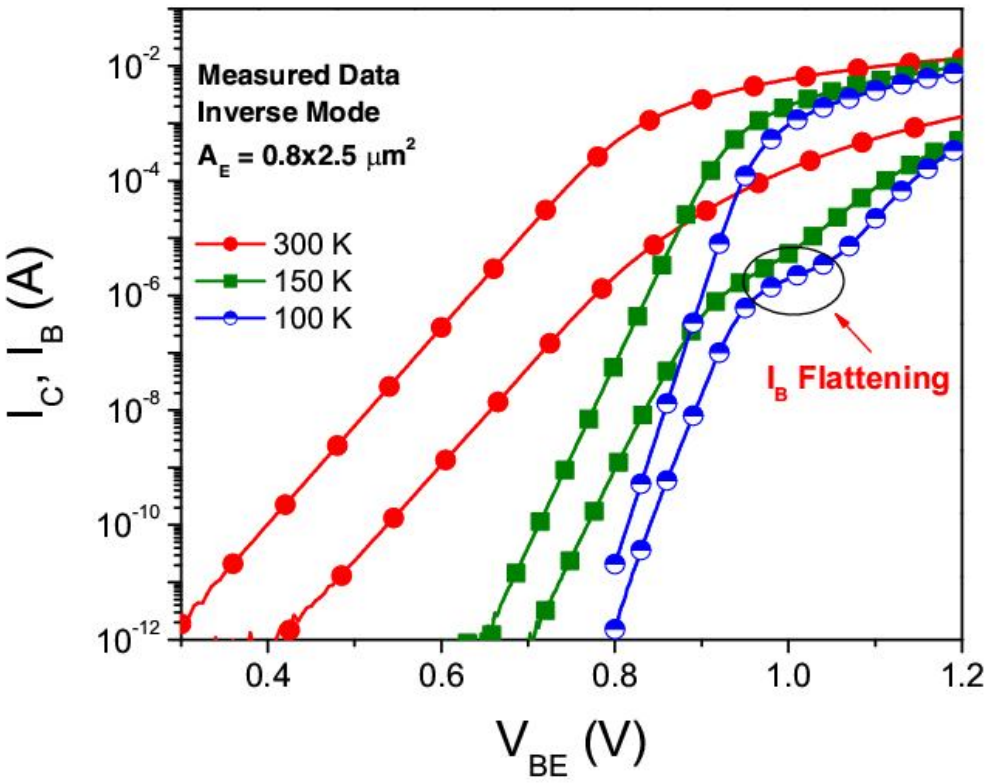


Figure 52. Inverse Gummel characteristics of a third generation SiGe HBT as a function of temperature.

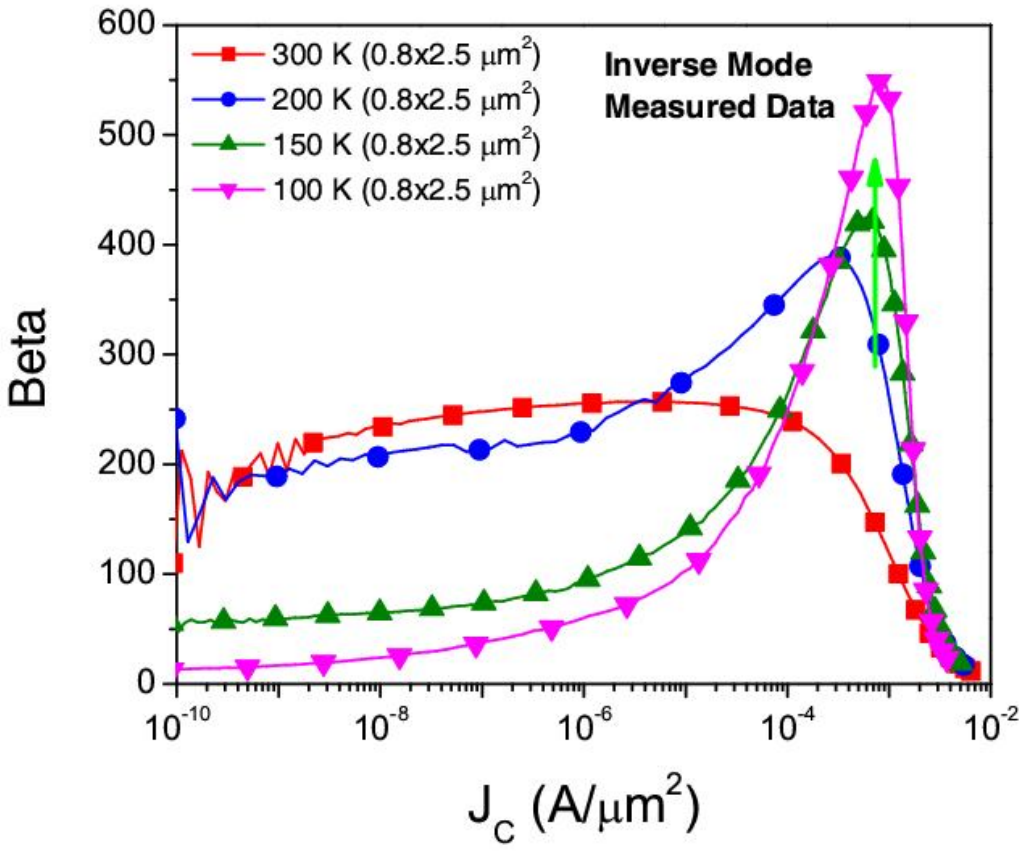


Figure 53. Inverse mode current gain of a third generation SiGe HBT as a function of temperature.

This behavior of the inverse mode gain is observed in the second-, third- and fourth-generation SiGe HBTs, for multiple devices, at temperatures below 200K. A closer examination of the inverse Gummel characteristics at reduced temperature reveals a base current "flattening" at high injection, which leads to the observed dramatic increase in gain.

To understand the unusual base current behavior, we simulated a SiGe HBT with a typical doping profile and a simple triangular Ge profile with varying peak germanium values. For a peak Ge concentration of 25%, we observe both the decrease in inverse mode current gain at the low-to-medium injection regime, and the flattening of the base current at high injection (Figure 54).

Interestingly, we observe that the base current flattening disappears when the recombination is selectively eliminated in the base by increasing the SRH lifetime. Eliminating recombination also dramatically improves the gain in the low- to-medium injection regime.

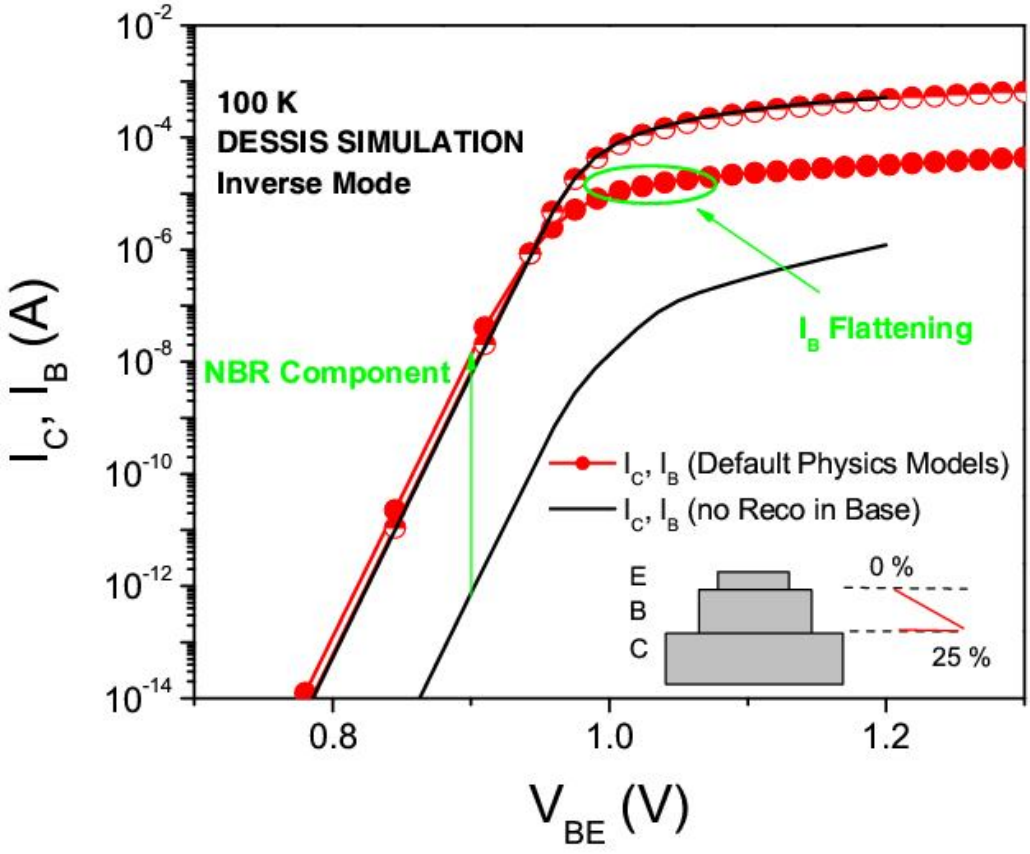


Figure 54. Simulated inverse mode Gummel at 100K for a SiGe HBT with a triangular profile (25% peak Ge) with and without recombination in the base.

Furthermore, a simulation of the same device at 300K does not show the unique base current behavior and eliminating base recombination does not influence the simulated inverse Gummel characteristics at all (Figure 55). Simulating a similar device structure at 100K, but with a 10% peak germanium, also does not show any base current flattening. The above facts therefore

suggest the temperature activated nature of the physics that leads to both increased recombination and hence the base current “flattening”.

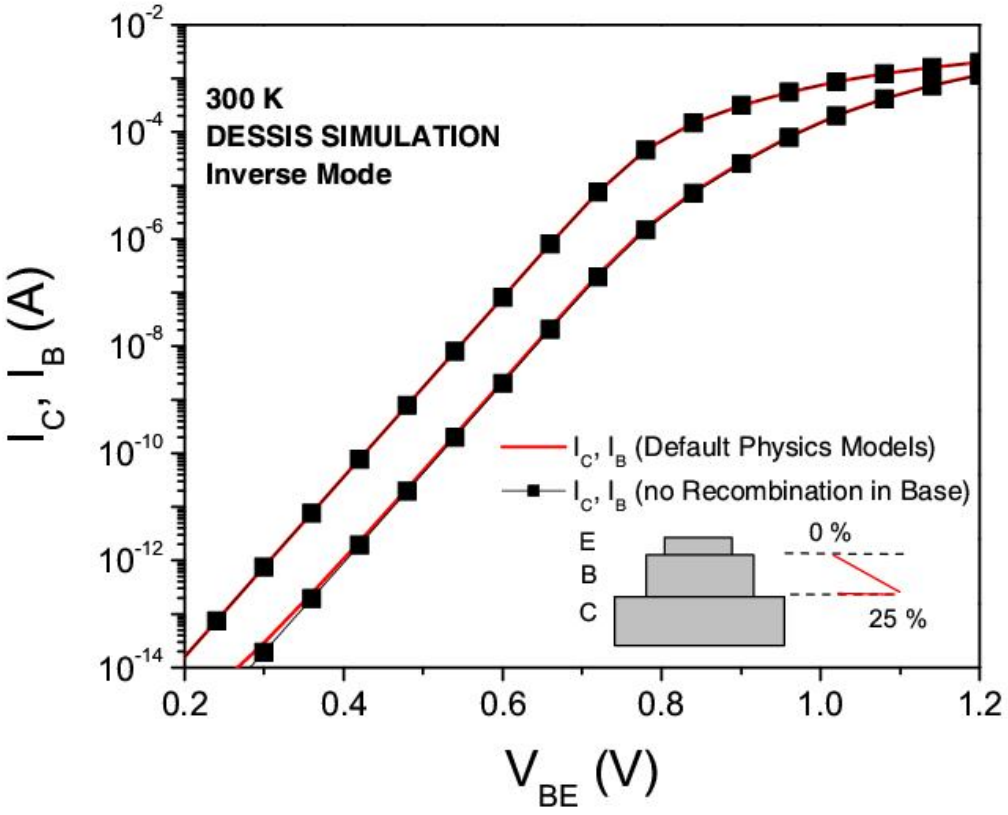


Figure 55. . Simulated inverse mode Gummel at 300K for a SiGe HBT with a triangular profile (25% peak Ge) with and without recombination in the base.

Shown in Figure 56 is the simulated electron current density contours for the inverse mode operation at 300K and 100K at low injection, through a region in the collector of the device close to the physical CB junction. As is clearly seen, the electron current density flows predominantly through the center of the device at 300K but is distributed evenly across the collector at 100K. The increased spread of the electron current at lower temperatures is due to the influence of the negative electric field in the base region in the inverse mode (due to Ge grading), which causes the electrons to diffuse in the lateral direction. The impact of the negative electric field is a strong

function of both the temperature and the peak Ge concentration, getting stronger at lower temperatures. The electrons that flow through the extrinsic portion of the device recombine in the extrinsic base region and therefore increase the base recombination current, leading to the decreased current gain at low-to-medium injection. This extrinsic recombination component is also independent of V_{CB} and therefore cannot be seen in the output characteristics.

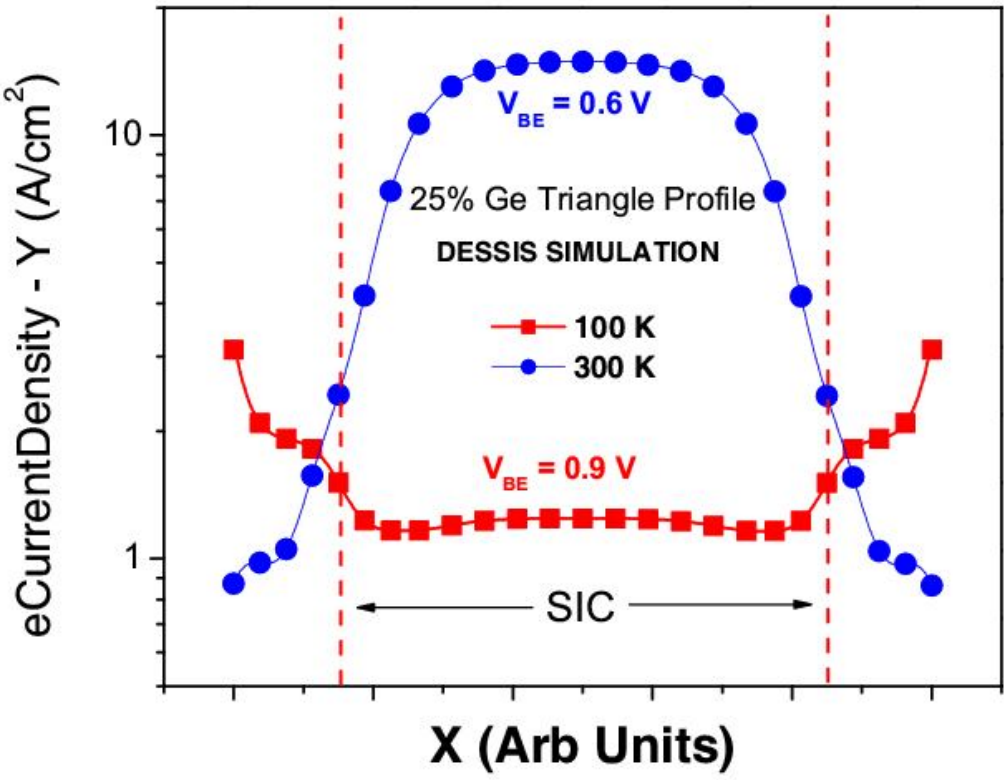


Figure 56. Electron current density contour along a horizontal cross section in the collector at 300K and 100K at medium injection.

Shown in Figure 57 is the simulated electron current density contour at 100K for the SiGe HBT with a 25% peak Ge at high injection. The electron current contour changes from a uniform lateral flow to being confined in the intrinsic portion of the device as seen at 300K. The onset of the heterojunction barrier effect at the physical CB junction causes increased charge accumulation

in the base which modifies the retarding electric field in the base, leading to the change in electron current contour (Figure 58). This confinement of the electron current removes the recombination base current component, thereby causing the observed dramatic improvement in current gain. The subsequent roll-off in gain is a result of high injection effects in the physical CB junction.

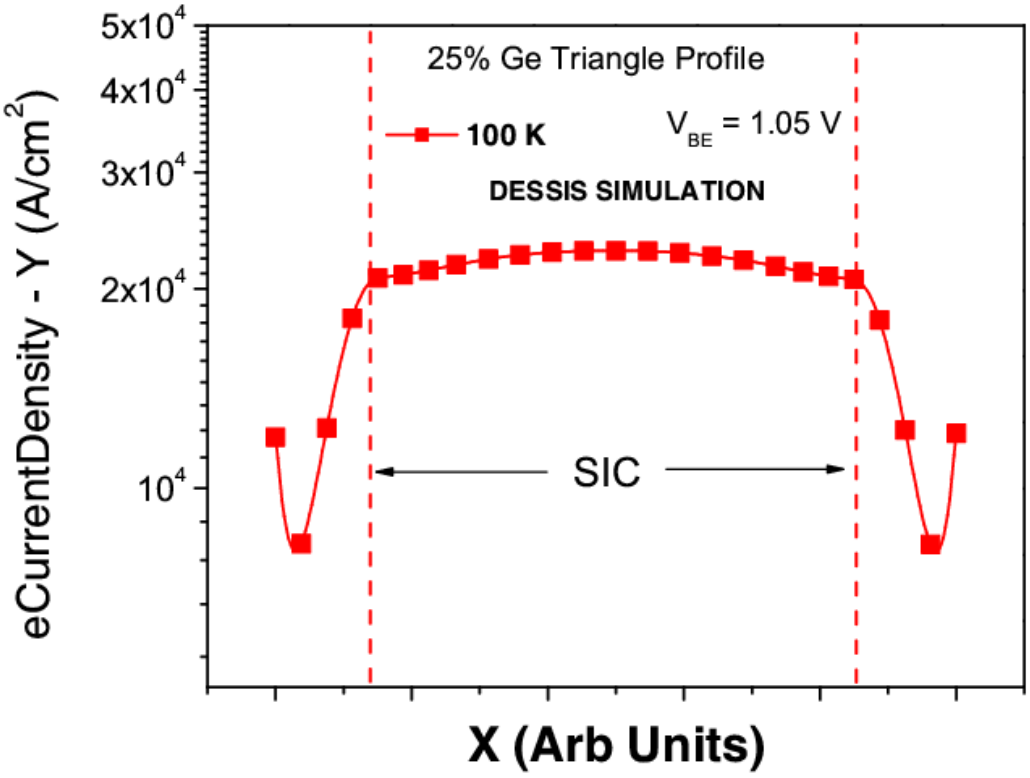


Figure 57. Electron current density contour along a horizontal cross section in the collector at 300K and 100K at high injection.

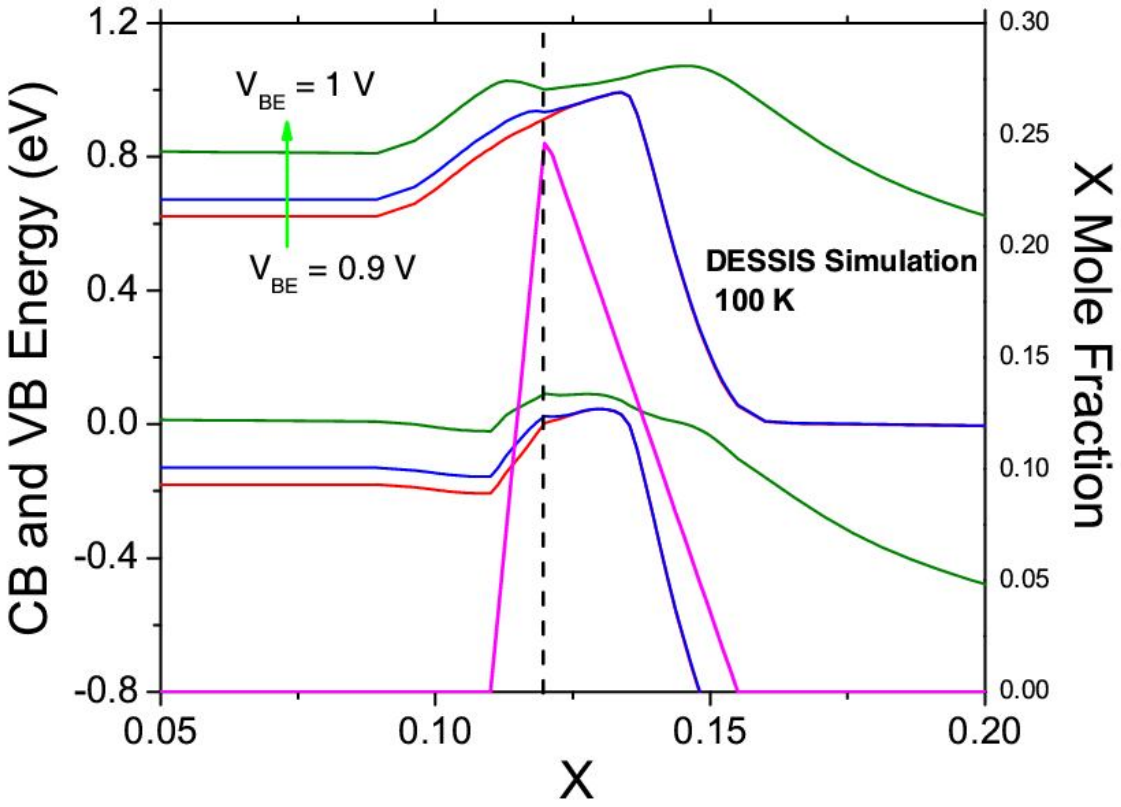


Figure 58. Conduction and valence band energy of SiGe HBT with a flipped Germanium profile. The device is simulated at 100 K at different injection levels. The loss of the retarding electric field is clearly seen from the band energies at high injection.

To further confirm this hypothesis, the device was also simulated by reversing the Ge triangle, so that the inverse mode of operation now sees an accelerating field and the forward mode sees a retarding field. As can be seen in Figure 59, this leads to a base current flattening behavior in the forward mode and not in the inverse mode, as expected. Furthermore, an examination of the current contours reveals increased electron current spreading in the forward mode and confined electron flow in the inverse mode.

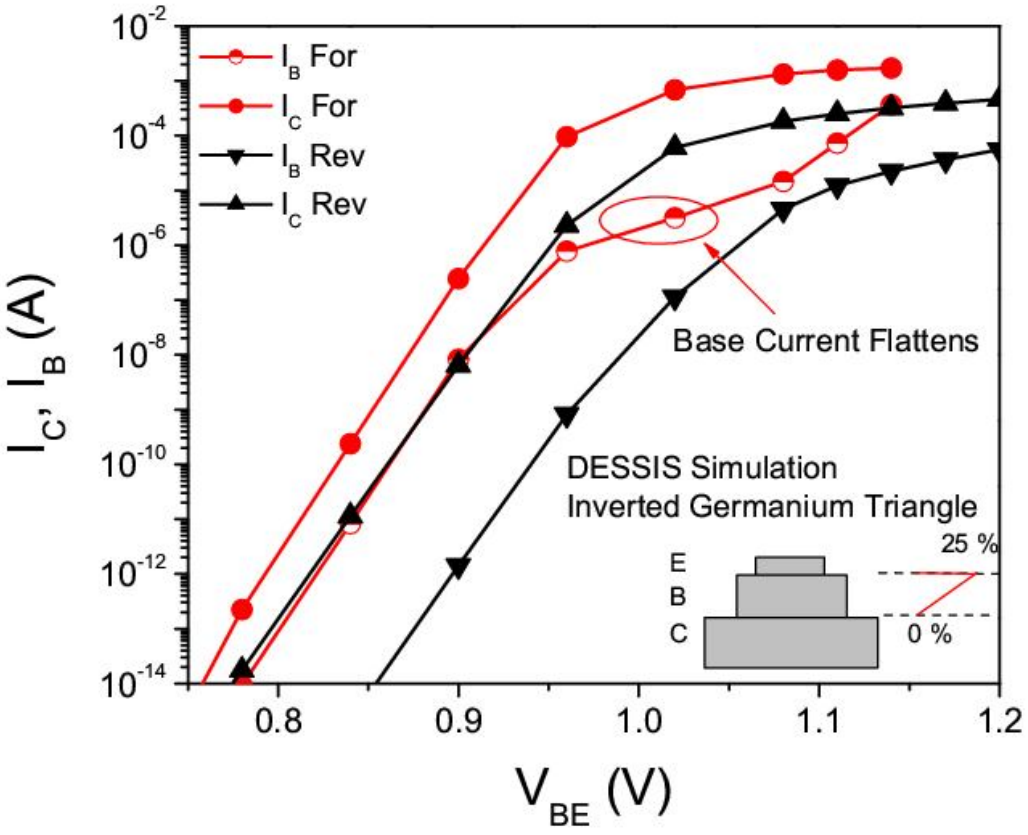


Figure 59. Simulated inverse and forward mode Gummel at 100K for a SiGe HBT with an inverted triangular profile (25% peak Ge).

The elimination of the extrinsic base current component leads to an increase in f_T of the device at lower temperatures at high current densities (Figure 60). Since the base transit time (τ_b) in the inverse mode is the limiting transit time at room temperature [9] and gets worse at reduced temperatures, we expect τ_b to dominate the total transit time at low temperatures. The increase in f_T at high injection might therefore be due to the decrease in the retarding field at high injection and the consequent decrease in minority charge storage in the extrinsic regions of the base.

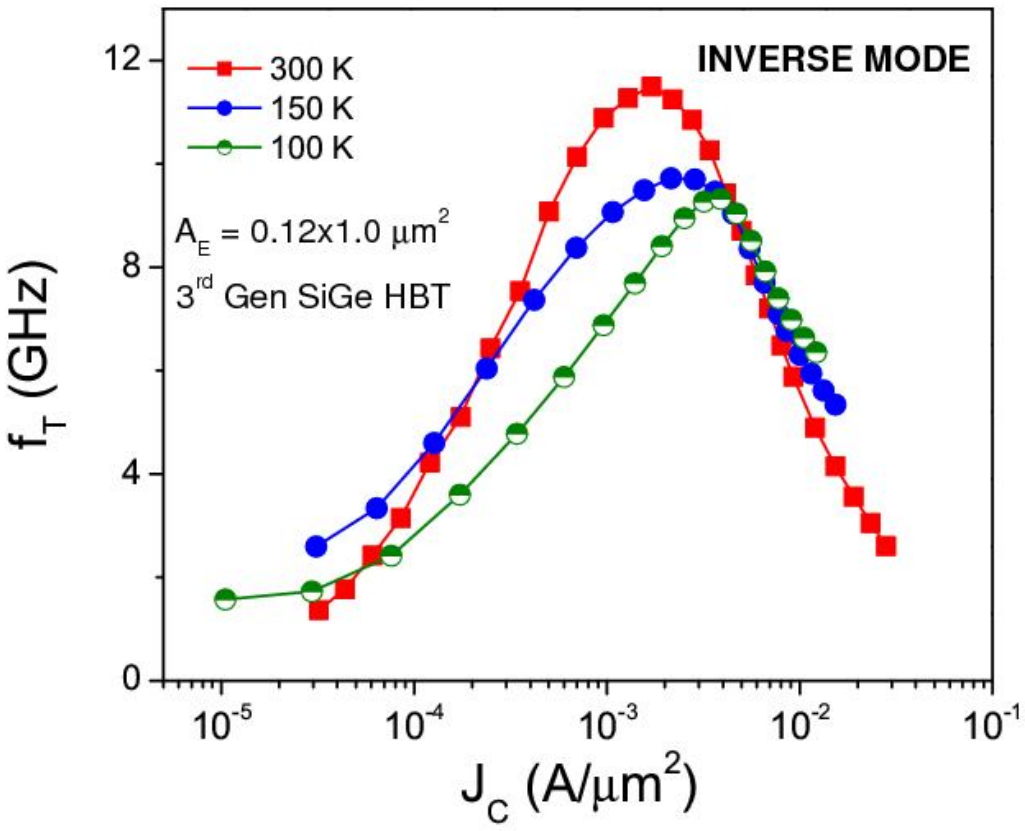


Figure 60. Measured inverse mode f_T as a function of collector current density at various temperatures.

The fact that the peak f_T in inverse mode operation does not degrade with cooling is clearly good news from an extreme environment application perspective. Inverse mode SiGe HBTs are therefore strong candidates for extreme environment applications considering their cryogenic performance and radiation hardness.

Chapter 5

Cryogenic Matching Performance of 90nm MOSFETs

As discussed previously, the cost advantage of SiGe HBT technology is tied to the possibility of integrating high performance SiGe HBTs with highly scaled CMOS devices for a true system-on-a-chip integration of digital, analog, and RF blocks. While SiGe HBTs, in both the forward and inverse mode of operation, have been shown to perform well at cryogenic temperatures, the performance of scaled CMOS devices in extreme environments also needs to be examined to ensure reliable system performance. In chapter 1, the TID tolerance of scaled CMOS devices was discussed. The examined 90nm technology was found to be radiation hard to a variety of radiation particles at large total dose. In this chapter, we examine the matching properties of nMOSFETs from a 90nm bulk technology platform across temperature.

5.1 Matching Performance

Device matching is an important metric that determines the performance of many critical analog circuit blocks like differential pairs, current mirrors, bandgap references and feedback networks [49]. Due to limitations imposed by fabrication, there are non-negligible differences in process parameters across the wafer and between wafer lots. For a MOSFET, this includes variations in gate oxide thickness and gate lengths, which lead to significant differences in die-to-die performance. To mitigate the effect of variability across the wafer, circuits are designed to operate using differential input on two closely placed transistors. Since closely spaced transistors enjoy similar processing conditions, their device-to-device variation is significantly smaller than the die-to-die difference making differential circuits the circuit of choice for precision analog

applications. With generational scaling, however, variability between closely spaced MOSFETs have increased significantly due to many factors like line-width variation in ultra-small gate length devices, gate polysilicon doping variations [50], and random dopant fluctuations in channel doping [51]. In ultra-scaled CMOS devices, device mismatch is dominated by random dopant fluctuations (RDF), which is caused due to the finite number of dopants in a MOSFET channel. The variability due to RDF is inversely proportional to the device area, and can therefore be reduced by using devices with a larger gate area. This approach however, leads to a tradeoff in chip size, parasitics (and therefore performance) and power consumption. In addition, for a fixed drain current, employing larger device widths often leads to operation of the MOSFETs in weak to moderate inversion where the effect of variability is enhanced [49].

The fundamental nature of the mismatch and its exacerbation with scaling has resulted in extensive investigations of the matching performance of scaled CMOS devices over the last two decades [49, 51]. While the matching properties of MOSFETs have been extensively studied, the impact of temperature on matching remains poorly understood. Recent efforts at understanding the effects of temperature on matching [52, 53] report improved matching at higher temperatures. Here, we examine the impact of cryogenic temperatures on the matching performance of a 90 nm bulk CMOS technology.

Cryogenic operation improves many of the MOSFET performance metrics and cryogenic MOSFETs have been shown to achieve lower broadband noise at cryogenic temperatures [54], opening up the possibility of their application in radio astronomy that require very low noise. As suggested in [52], however, device matching could potentially degrade with cooling. In addition to the enhancement of columbic scattering and the associated variations due to dopant

fluctuations [53], cryogenic temperatures impose additional variability due to incomplete ionization and enhanced quantum effects.

In this work, nMOSFETs of multiple dimensions were layed-out in a common source/body configuration with separate drain and gate contacts. To conserve space, four devices of identical dimensions were placed at minimum distance from each other, constituting six identical device pairs (Figure 61). The devices to be measured were selected by the gate and drain biases. Linear transfer characteristics were measured at a drain-to-source voltage (V_{DS}) of 50 mV at a body bias of 0 V and -0.6 V. Threshold voltages were extracted using the constant current method at multiple fixed drain currents. A set of 30 device pairs was measured to ensure adequate statistics.

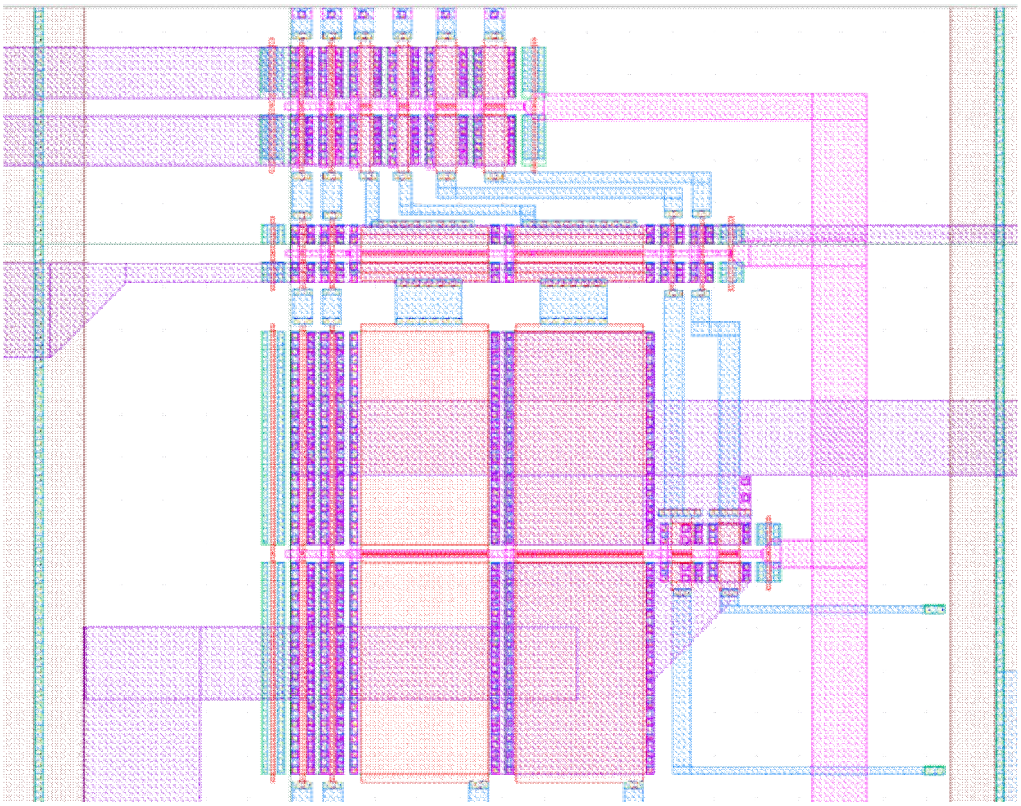


Figure 61. Layout of matching transistor array

The normalized peak transconductance (g_m) of discrete nMOSFETs of multiple device dimensions from the same technology node, as a function of temperature, is shown in Figure 62. As expected, the peak transconductance improves with cooling due to the improvement in mobility. In addition, MOSFETs with larger gate length show a larger improvement in peak g_m due to their lower channel doping.

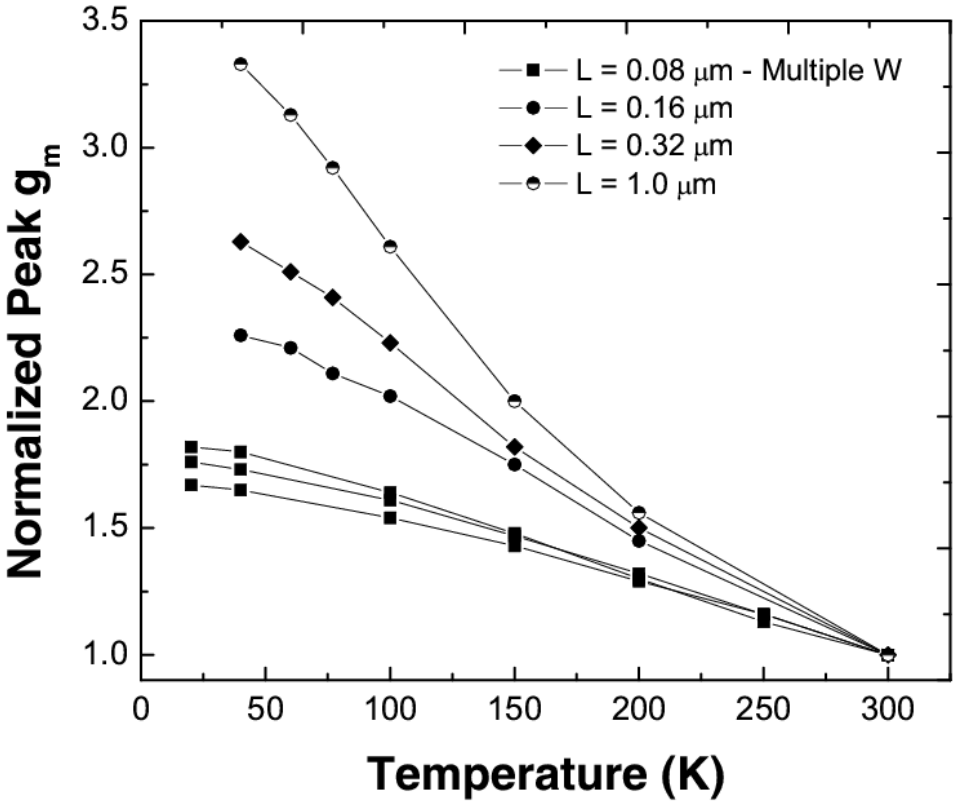
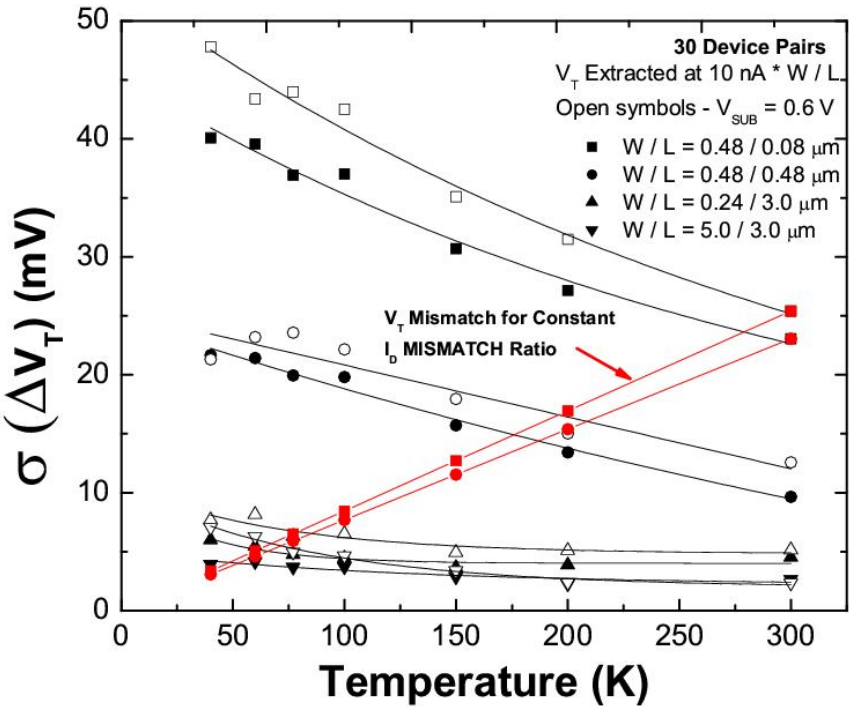


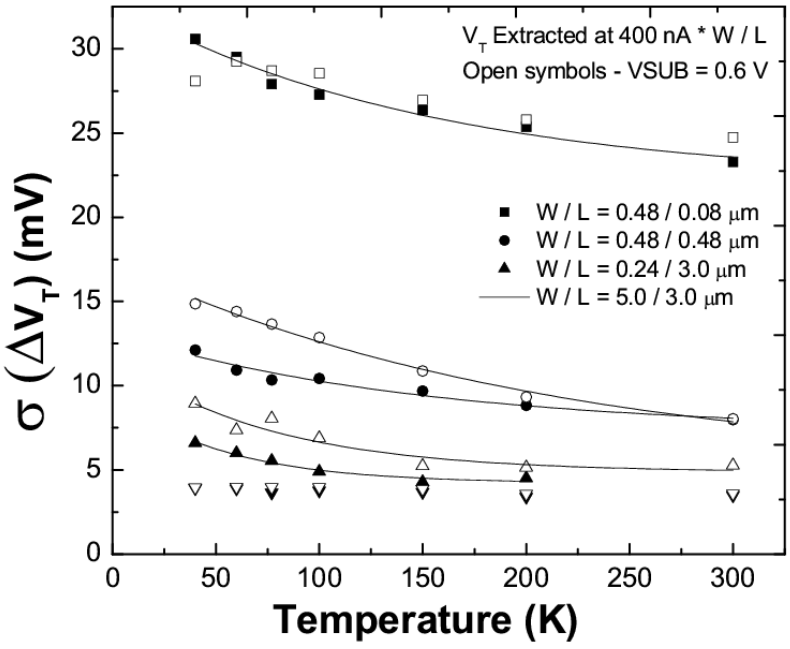
Figure 62. Normalized transconductance as a function of temperature. The transconductance is normalized to the value at 300K

The mismatch in threshold voltage (V_T) for three fixed drain currents (I_D) is shown in Figure 63. The V_T mismatch decreases with increasing device dimensions (as expected) and increases with cooling (not as expected). Interestingly, the temperature sensitivity of the mismatch is a function of the drain current at which V_T is extracted, and the temperature

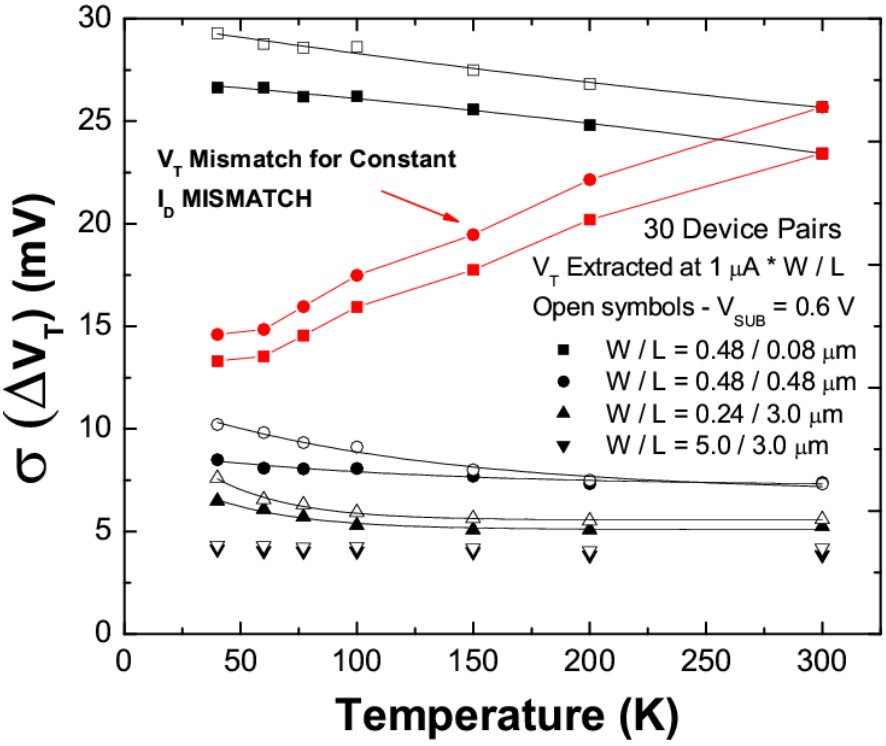
sensitivity decreases with increasing drain currents. In addition, the mismatch worsens with increasing substrate bias.



(a)



(b)



(c)

Figure 63. V_T mismatch as a function of temperature extracted at three different drain currents (a) 10nA, (b) 400nA, and (c) 1 uA

Since current mismatch is a more relevant metric for many circuit applications, we have also included the V_T mismatch for constant I_D mismatch across temperature in Figure 63. For the same drain current ratio in subthreshold, the threshold voltage mismatch can be expressed as (assuming identical body factor across temperature):

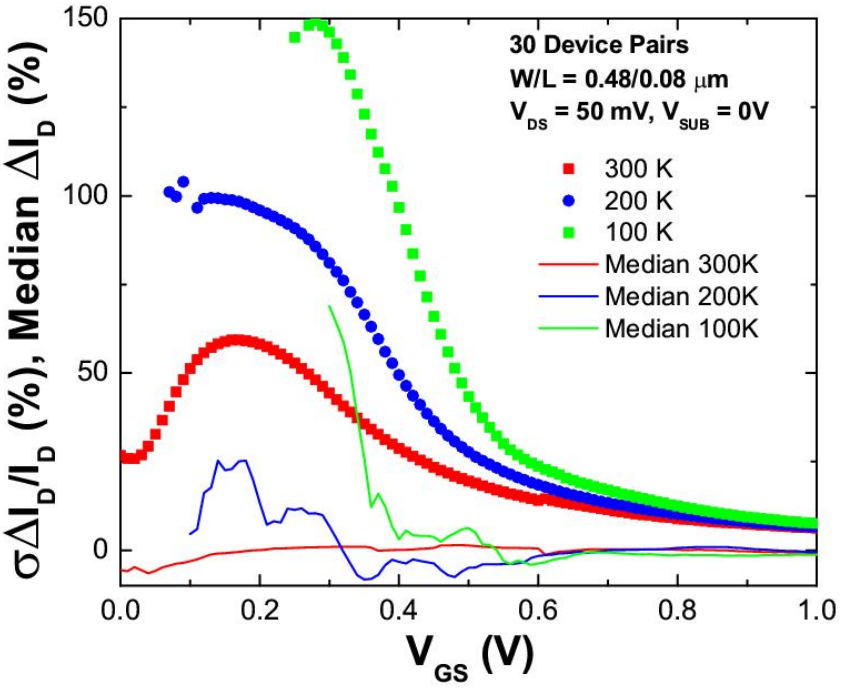
$$\Delta V_T(T) = \Delta V_T(300K).\frac{T}{300} \quad (1)$$

Under strong inversion, for the same drain current mismatch, the required threshold voltage mismatch can be expressed as:

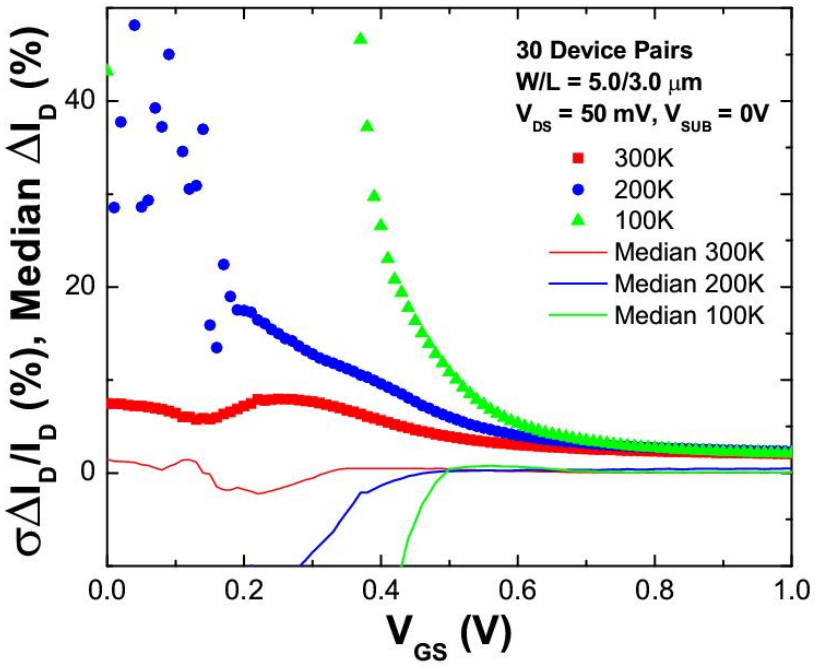
$$\Delta V_T(T) = \Delta V_T(300K).\frac{\mu(300)}{\mu(T)} \quad (2)$$

The more stringent requirement for threshold voltage matching with cooling is due to the improved subthreshold swing and higher mobility at low temperatures. Here, we determine the ratio of the mobility across temperature from the measured transconductance (Figure 62).

The drain current mismatch as a function of gate source voltage is shown in Figure 64. As observed in [1], the drain current mismatch decreases with increasing V_{GS} and is largely invariant across temperature at $V_{GS} = V_{DD}$ (Figure 65). This suggests a dopant number fluctuation induced mismatch [55]. Additionally, the median I_D mismatch is significantly smaller than the absolute I_D mismatch, which illustrates the random nature of the mismatch [56]. While the V_T mismatch for the large device (W/L = 5.0/3.0 μm) is invariant across T, the drain current mismatch increases significantly in the subthreshold region, which is a concern for ultra-low power circuit operation at cryogenic temperatures.



(a)



(b)

Figure 64. Drain current mismatch as a function of gate voltage for two devices (a) W/L = 0.48/0.08 and (b) 5.0/3.0 um

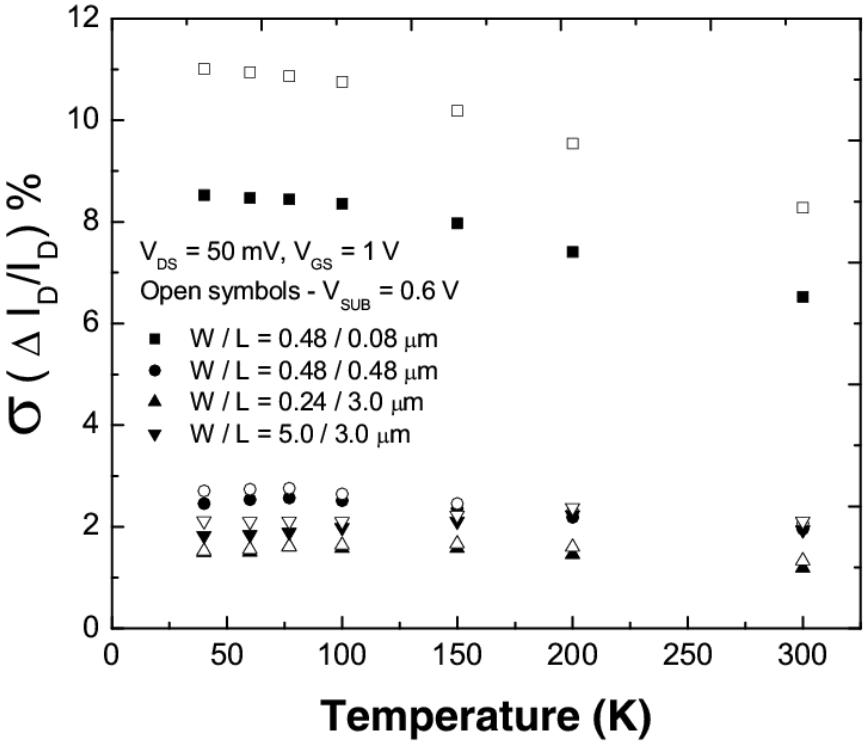


Figure 65. Drain current mismatch ratio at $V_{GS} = V_{DD}$ as a function of temperature.

5.2 Discussion

While the temperature dependence of mismatch has been observed earlier, the underlying physics behind the mismatch behavior across temperature is not entirely clear. The increasing influence of impurity scattering at reduced temperature is suggested as the reason for the increased variability in mobility (and therefore current) with cooling in [52]. While we do observe the increase in drain current mismatch at $V_{GS} = V_{DD}$ (the bias range most sensitive to mobility mismatch), the increasing impurity scattering alone does not fully explain the mismatch behavior at cryogenic temperatures. In our samples, the drain current mismatch decreases as a function V_{GS} while a purely mobility driven mismatch would imply a constant I_D mismatch across V_{GS}.

TCAD simulations are used here to understand the influence of temperature on mismatch. A typical 90nm nMOSFET structure is created using process simulations and compared to a similar device with a 20% difference in a chosen process parameter. The process uses four implants for defining the channel region, halo implants for controlling short channel effects and a constant poly-silicon gate doping. No mechanical strain is introduced in the device. Multiple transistor structures are created by changing process parameters including the dose/energy of the channel and halo implant, gate length, and gate doping concentration. Device simulations are subsequently run at 300K and 125K. The Philips unified mobility model is used to include the effect of temperature and vertical fields on mobility and the channel quantization is modeled using the density gradient model. Incomplete ionization was found to have no significant influence on the mismatch behavior across temperature.

The effect of different process parameters on the V_T mismatch as a function of temperature is shown in Figure 66. Variation in the halo dose causes the most significant change in threshold voltage as observed in [51]. The mismatch due to process variations is, however, insensitive to temperature. Changing the temperature from 300K to 125 K results in less than a 10% change in V_T mismatch for all the process parameters examined here.

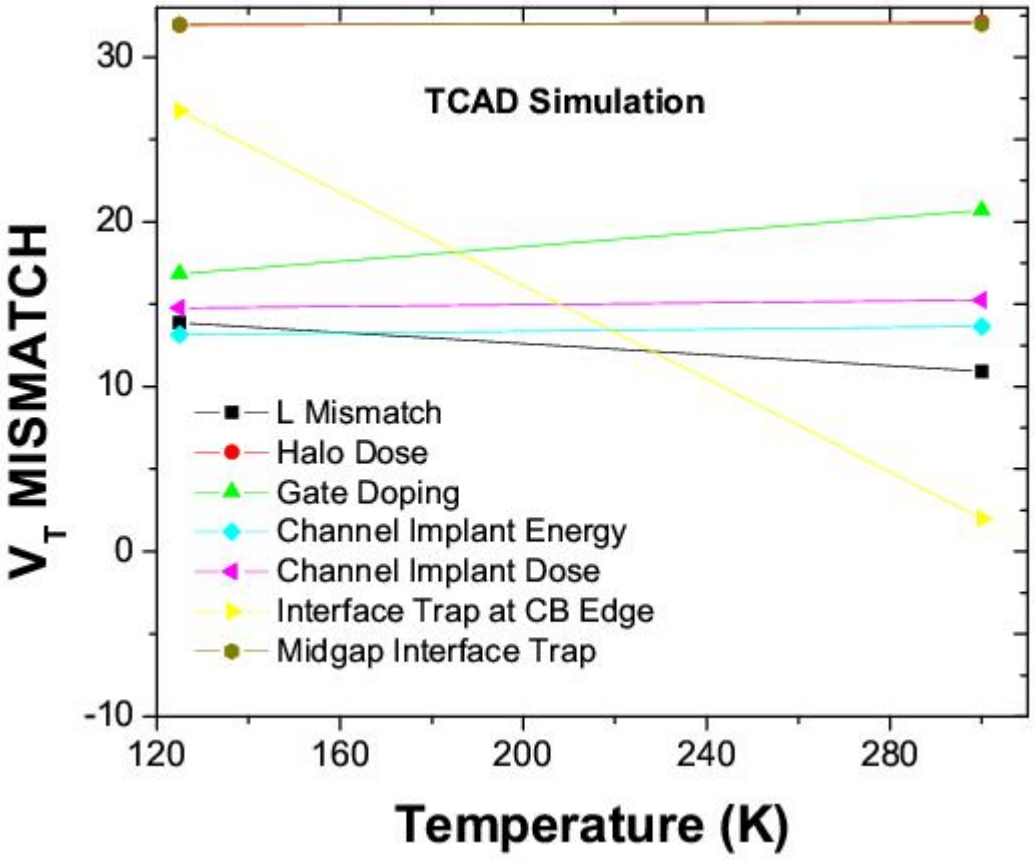


Figure 66. Change in V_T mismatch as a function of process parameters and temperature.

The presence of interface traps, however, dramatically increases the temperature sensitivity of V_T mismatch. The V_T mismatch increases from 1 mV at 300K to 27 mV at 125K. Here, acceptor traps with a concentration of $4*10^{11}$ cm^{-2} at a single energy level are introduced

near the conduction band edge. It is to be noted that the temperature sensitivity of mismatch due to interface traps is a function of the interface trap energy. For traps with energy predominantly near the middle of the silicon bandgap, the threshold voltage shift is insensitive to temperature, while mismatch in devices with traps close to the conduction band edge are highly sensitive to temperature.

The simulated transfer characteristics of a 90nm MOSFET as a function of temperature and interface trap energy is shown in Figure 67. The interface traps near the conduction band edge in nMOSFETs has been shown to be acceptor type traps [57] and therefore, only acceptor type traps are investigated in this work. It is to be noted that the acceptor type traps are neutral when unoccupied and become negatively charged when filled with an electron. The added negative charge causes an increase in threshold voltage in nMOSFETs. At room temperature, the presence of acceptor traps at the conduction band edge leads to a degradation in transconductance but a negligible shift in threshold voltage. This is because, the bias (V_{GS}) at which the traps get filled with electrons correspond to the moderate inversion region at room temperature. At cryogenic temperature however, the traps get filled when the device is biased in the subthreshold region of operation (due to decreasing n_i) causing a threshold voltage shift. The "transition" voltage at which the traps become occupied is a function of the trap energy. At low enough energy (near the mid-gap), the traps are occupied at zero gate bias which leads to a pure threshold voltage shift at room temperature; the V_T mismatch in this case also becomes insensitive to temperature. For traps near the conduction band edge, the apparent shift in threshold voltage at cryogenic temperature due to interface traps causes the increase in threshold voltage mismatch at cryogenic temperatures. A classical behavior of the effect of interface traps on matching is shown in Figure 68. The energy distribution of interface traps also explains the

behavior of V_T mismatch as a function of current. At high I_D (under strong inversion), all the traps are filled at room temperature as well as cryogenic temperature, leading to a constant mismatch across temperature. At low currents however, traps are occupied only at cryogenic temperatures leading to a significantly higher mismatch at cryogenic temperatures.

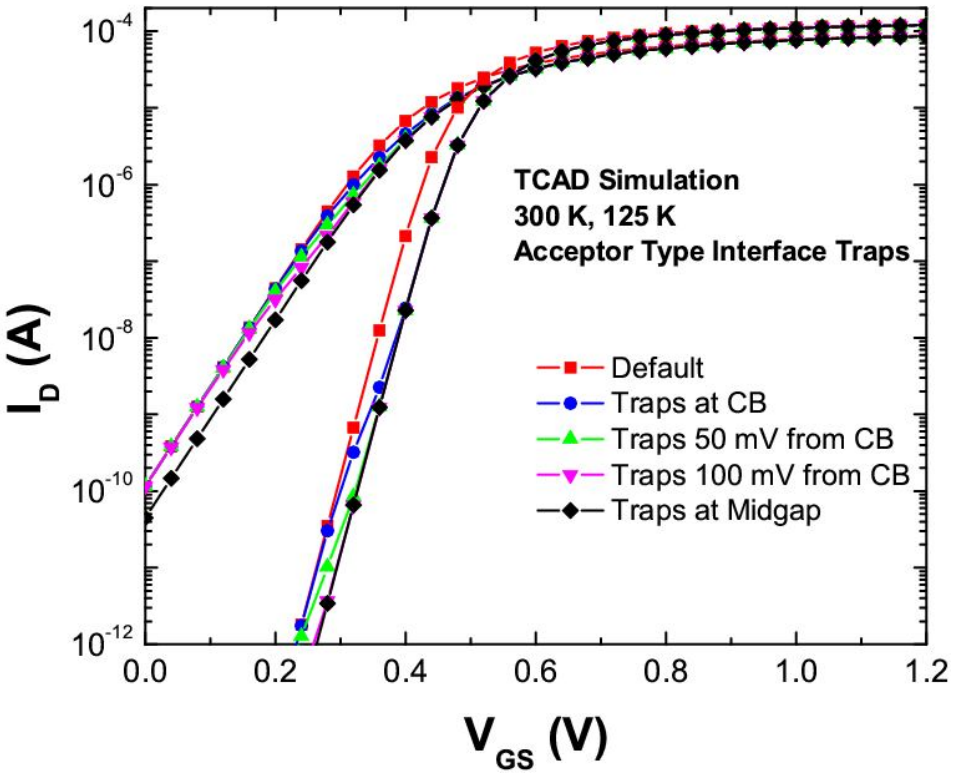


Figure 67. Drain currents as a function of interface trap energy and temperature

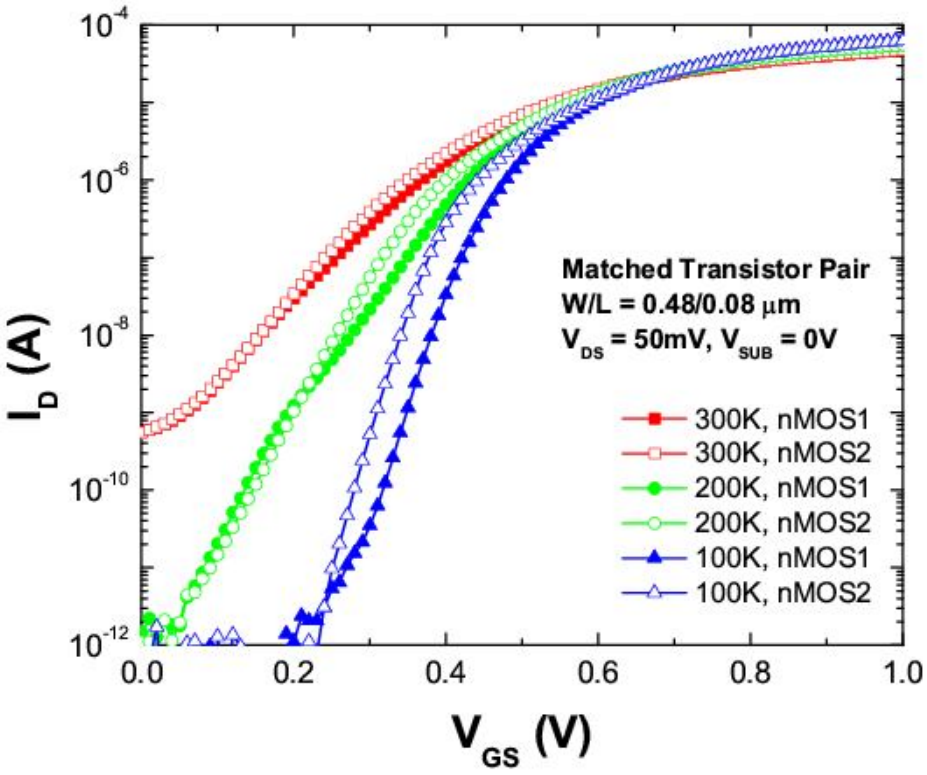


Figure 68. Measured transfer characteristics of a matched transistor pair as a function of temperature

The influence of interface traps on the matching characteristics of MOSFETs implies that MOSFETs biased in subthreshold region are more vulnerable to hot carrier stress effects at cryogenic temperature as compared to room temperature. For example, shown in Figure 69 are the transfer characteristics of a 150nm gate length nMOSFET manufactured in a 65 nm SOI technology platform as a function of temperature. The device was initially stressed at 77K at a V_{GS} = 2.25V and V_{DS} = 2.4 V. The threshold voltage in the subthreshold region increases with stress time due to an increase in interface trap creation. After 1000s of stress, the device was measured at room temperature. As expected from the previous discussion, the degradation in transfer characteristics at room temperature get manifested as a subthreshold slope degradation. Interestingly, when subsequently cooled to 77K again, the threshold voltage shift is seen to

decrease implying spontaneous annealing at room temperature. Also, one can observe that the degradation at 77K, remains as a pure V_T shift in the subthreshold region.

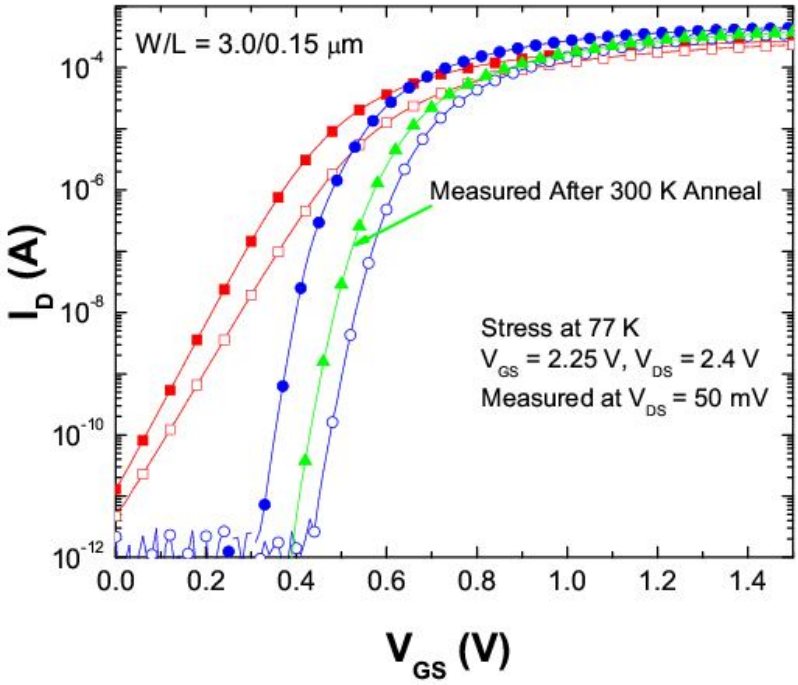


Figure 69. Measured transfer characteristics of a 150nm gate length SOI nMOSFET. The device is stressed at 77K, then measured at 300K and subsequently measured at 77K again.

A plot of the threshold voltage change with stress as a function of drain current at 300K and 77K reveals the effect of temperature on V_T mismatch due to interface traps (Figure 70). At low drain currents, the threshold voltage is degraded significantly more at 77K as compared to 300K. With increasing drain current however, this difference decreases. TCAD simulations (Figure 71) confirm the influence of interface traps on the current degradation with stress across temperature.

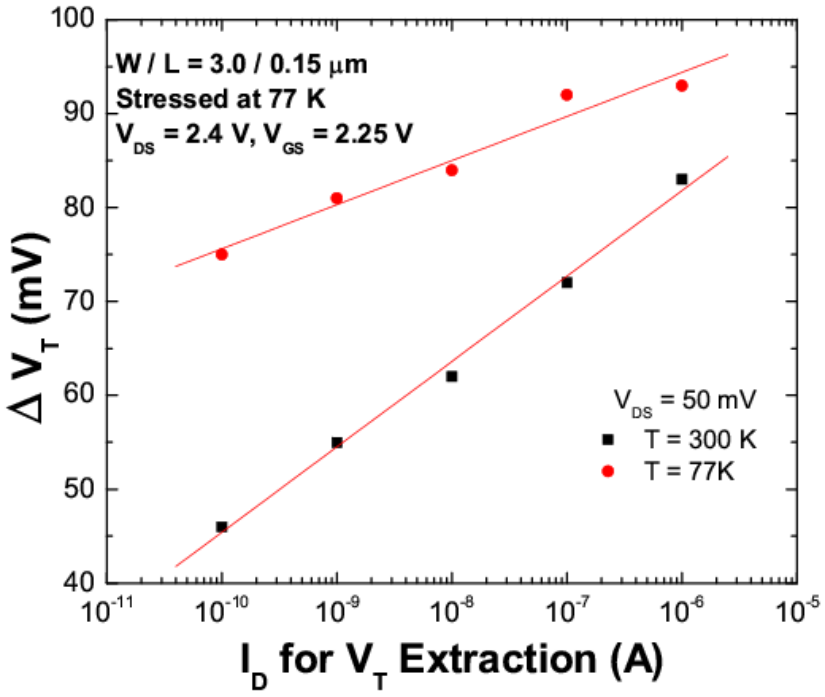


Figure 70. Threshold voltage shift with stress as a function of the drain current at which threshold voltage is extracted.

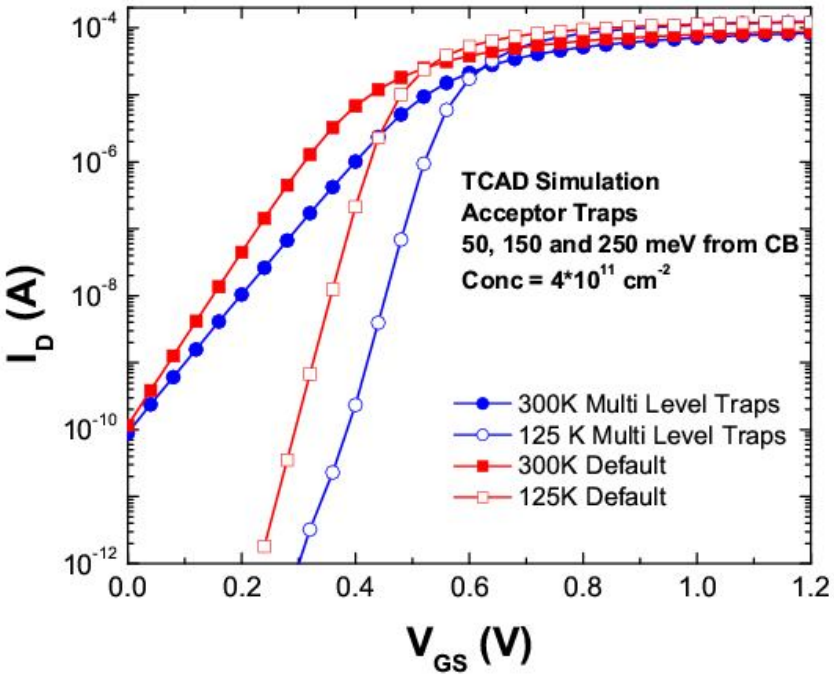


Figure 71. Simulated transfet characteristics of nMOSFETs with interface traps placed at 50, 150 and 250 meV from conduction band edge.

Chapter 6

Conclusion and Future Work

The goal of this work was to examine SiGe HBTs and scaled CMOS devices in the context of extreme environments. The following sections summarize my contributions towards the same and describe future directions of research.

6.1 Contributions

1. Proposed inverse mode operation as a viable SEU hard design in SiGe HBT technology.
2. Examined the impact of scaling on the inverse mode operation of SiGe HBTs and identified the performance limitations in inverse mode.
3. Layed out optimized device structures that show a 300% improvement in measured inverse mode peak f_T. These improvements were made using no process modifications.
4. Proposed a new cascoded device structure that combines the performance of forward mode SiGe HBTs with the radiation hardness of inverse mode operation.
5. Examined the cryogenic operation of inverse mode SiGe HBTs. Here, a new base current phenomenon at high injection was identified that has implications on inverse mode performance at cryogenic temperatures.
6. Examined the TID tolerance of 90nm strained silicon CMOS technology. The tolerance of process induced strain to displacement damage was demonstrated in this work for the first time.

7. Investigated the matching performance of 90nm bulk nMOSFETs at cryogenic temperatures. The effect of interface traps on the subthreshold current matching is demonstrated in this work.

6.2 Future Work

1. Develop a compact model incorporating all the physics of inverse mode operation.
2. Develop ring oscillators using optimized inverse mode SiGe HBTs and examine their peak performance.
3. Examine the SEU hardness of shift registers designed using inverse mode SiGe HBTs.
4. Examine the SEU hardness of shift registers designed using inverse cascode devices.
5. Examine the cryogenic operation of optimized inverse mode SiGe HBTs.
6. Investigate the matching characteristics of low V_T MOSFETs.
7. Investigate optimized lay outs for improving cryogenic matching performance.
8. Investigate the matching performance of SiGe HBTs at cryogenic temperatures through a mix of measurements and simulations.
9. Investigate the reliability of scaled CMOS devices in extreme environemts. It would also be interesting to examine the impact of stress on matching performance.

REFERENCES

[1]. J. D. Cressler, "On the potential of SiGe HBTs for extreme environment electronics," *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1559-1582, 2005.

[2]. J. D. Cressler, and G. Niu , Silicon-Germanium heterojunction bipolar transistors. Boston: Artech House, 2003.

[3]. M. Turowski, A. Raman, and R. D. Schrimpf," Nonuniform total-dose-induced chare distribution in shallow trench isolation oxides," IEEE Transactions on Nuclear Science, vol. 51, no. 6, pp. 3166-3171, 2004

[4]. P. W. Marshall, M. A. Carts, A. Campbell, D. Mcmorrow, S. Buchner, R. Stewart, B. Randall, B. Gilbert, and R. A. Reed, "Single-event effects in circuit-hardened SiGe HBT logic at gigabit per second data rates," *IEEE Transactions on Nuclear Science*, vol. 47, no. 6, pp. 2669-2674, Dec. 2000.

[5]. G. E. Schwarze, A. J. Frasca," Neutron and Gamma irradiation effects on power semiconductor switches," *Proceedings of the 25th Intersociety Energy Conversion Engineering Conference*, vol. 6, pp. 30-35, 1990.

[6]. B. S. Meyerson," UHV/CVD growth of Si and Si:Ge Alloys: Chemistry, physics, and device applications," *Proceedings of the IEEE*, vol. 80, n0. 10, pp. 1592-1608, 1992

[7]. D. C. Ahlgren, G. Freeman, S. Subbanna, R. Groves, D. Greenberg, J. Malinowski, D. Nguyen-Ngoc, S. J. Jeng, K. Stein, K. Schonenberg, D. Kiesling, B. Martin, S. Wu, D. L. Harame, and B. Meyerson, "A SiGe HBT BiCMOS technology for mixed signal RF applications," in *Proc. BCTM*, 1997, pp. 195-197.

[8]. G. Freeman, D. C. Ahlgren, D. R. Greenberg, R. Groves, F. Huang, G. Hugo, B. Jagannathan, S. J. Jeng, J. Johnson, K. Schonenberg, K. Stein, R. Volant, and S. Subbanna, "A 0.18 μm 90 GHz f_T SiGe HBT BiCMOS, ASIC compatible, copper interconnect technology for RF and microwave applications," *IEDM Tech. Dig.*, 1999, pp. 569-572.

[9]. B. Jagannathan, M. Khater, F. Pagette, J.-S. Rieh, D. Angell, H. Chen, J. Florkey, F. Golan, D. R. Greenberg, R. Groves, J. Johnson, E. Megistsu, K. Schonenberg, C. M. Schnabel, P. Smith, A. Stricker, D. C. Ahlgren, G. Freeman, K. Stein, and S. Subbanna, "Self-aligned SiGe NPN transistors with 285 GHz f_{max} and 207 GHz f_T in a manufacturable technology," *IEEE Electron Device Letters*, vol. 23(5), pp. 258-260, 2002.

[10]. M. Khater, J.-S. Rieh, T. Adam, A. Chintakindi, J. Johnson, R. Krishnasamy M. Meghelli, F. Pagette, D. Sanderson, C. Schnabel, K.T. Schonenberg, P. Smith, K. Stein, A. Strieker, S.-J Jeng, D. Ahlgren, and G. Freeman, "SiGe HBT technology with

f_{max}/f_T = 350/300 GHz and gate delay below 3.3 ps," in *IEDM Tech. Dig.*, 2004, pp. 247-250.

[11]. G. Freeman, B. Jagannathan, S-J. Jeng, J-S. Rieh, A. D. Stricker, D. C. Ahlgren, and S. Subbanna, "Transistor design and application considerations for > 200 GHz SiGe HBTs," *IEEE Trans. Electron Devices,* vol. 50(3), pp. 645-655, 2003.

[12]. R. Krithivasan, Y. Lu, J. D. Cressler, J-S. Rieh, M. H. Khater, D. Ahlgren, and G. Freeman, "Half-Terahertz operation of SiGe HBTs," *IEEE Electron Device Letters*, vol. 27, no. 7, pp. 567-569, July 2006.

[13]. J. Yuan, J. D. Cressler, R. Krithivasan, T. Thrivikraman, M. H. Khater, D. C. Ahlgren, A. J. Joseph, and J-S. Rieh," On the performance limits of cryogenically operated SiGe HBTs and its relation to scaling for terahertz applications," *IEEE Transactions on Electron Devices*, vol. 56, no. 5, 2009.

[14]. A.K. Sutton, A. P.,Gnana Prakash, B. Jun, E. Zhao, M. Bellini, J. Pellish, R.M. Diestelhorst, M.A. Carts, A. Phan, R. Ladbury, J.D. Cressler, P.W. Marshall, C.J. Marshall, R.A. Reed, R.D. Schrimpf, and D.M. Fleetwood, "An Investigation of Dose Rate and Source Dependent Effects in 200 GHz SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3166-3174, June 2006.

[15]. Y. Taur and T. H. Ning, Fundamentals of modern VLSI devices, Cambridge: Cambridge university press, 1998.

[16]. S. T. Liu *et al.*, "Total radiation hard 0.35 μm SOI CMOS technology,"*IEEE Transactions on Nuclear Science*, vol. 45, no. 6, pp. 2442-2449, 1998.

[17]. S. E. Thompson *et al.*, "A 90 nm logic technology featuring strained silicon," *IEEE Transactions on Electron devices*, vol. ED-51, no. 11, pp. 1790-1797, 2004.

[18]. Y. Li, *et al*, "Proton radiation effects in 0.35-μm partially depleted SOI MOSFETs fabricated on UNIBOND,"*IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 2930-2936, 1998

[19]. J. Cai, *et al.*, "Performance comparison and channel length scaling of strained silicon FETs on SiGe-on-Insulator (SGOI)," *Proceedings of IEDM Technology Digest*, pp. 165-168, 2004.

[20]. H. S. Yang, *et al.*, "Dual stress liner for high performance sub-45 nm gate length SOI CMOS manufacturing," *Proceedings of IEDM Technology Digest*, pp. 1075-1077, 2004.

[21]. G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electronics Letters*, pp. 543-545, 1988.

[22]. C. M. Casteneda, "Crocker nuclear laboratory (CNL) radiation effects measurement and test facility," *Proc. Rad. Eff. Work.*, pp. 77-81, 2001.

[23]. P. W. Marshall, M. A. Carts, A. Campbell, D. Mcmorrow, S. Buchner, R. Stewart, B. Randall, B. Gilbert, and R. A. Reed, "Single-event effects in circuit-hardened SiGe HBT logic at gigabit per second data rates," *IEEE Transactions on Nuclear Science*, vol. 47, no. 6, pp. 2669-2674, Dec. 2000.

[24]. D. L. Hansen, P. Chu, and S. F. Meyer, "Effects of data rates and transistor size on single-event upset cross sections for InP based circuits," *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 3166-3171, Dec. 2005.

[25]. O. A. Amusan, A. F. Witulski, L. W. Massengill, B. L. Bhuva, P. R. Fleming, M. L. Alles, A. L. Sternberg, J. D. Black, and R. D. Schrimpf, "Charge collection and charge sharing in a 130 nm CMOS technology," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3253-3258, Dec. 2006.

[26]. M. Shoga, K. Jobe, M. Glasgow and M. Bustamante, "Single event upset at Gigahertz frequencies," *IEEE Transactions on Nuclear Science*, vol. 41, no. 6, pp. 2252-2258, Dec. 1994.

[27]. R. A. Reed, P. W. Marshall, J. C. Pickel, M. A. Carts, B. Fodness, G. Niu, K. Fritz, G. Vizkelethy, P. E. Dodd, T. Irwin, J. D. Cressler, R. Krithivasan, P. Riggs, J. Prairie, B. Randall, B. Gilbert, and K. A. LaBel, "Heavy-Ion Broad-Beam and Microprobe Studies of Single-Event Upsets in 0.20-µm SiGe Heterojunction Bipolar Transistors and Circuits," *IEEE Transactions on Nuclear Science*, vol. 50, no. 6, pp. 2184-2190, Dec. 2003.

[28]. H. T. Berger and S. K. Wiedman, "Merged-transistor logic (MTL) – a low cost bipolar logic concept," *IEEE Journal of Solid State Circuits*, vol. sc7(5), pp. 340-346, 1972.

[29]. H. Kroemer," Heterostructure bipolar transistors and integrated circuits," Proc. of the IEEE, vol. 70 (1), pp. 13-25, 1982.

[30]. S. Yamahata, Y. Matsuoka, and T. Ishibashi, "High-fmax collector-up AlGaAs/GaAs heterojunction bipolar transistors with a heavily carbon doped base fabricated using oxygen ion implantation," *IEEE Electron Device Letters*, vol. 14 (4), pp. 173-175, 1993.

[31]. C. B. Chen, Y. K. Su, et.al.," Fabrication of InGaP/Al0.98Ga0.02As/GaAs oxide-confined collector-up heterojunction bipolar transistors," *IEEE Electron Device Letters*, vol. 124 (10), pp. 619-621, 2003.

[32]. N. Matine, M. W. Dvorak, et.al.," InP in HBTs by vertical and lateral wet etching," *Proceedings of the International Conference on Indium Phosphide Related Materials*, pp 195 – 198, 1998.

[33]. A. Girardot, A. Henkel, et.al.," High performance collector-up InGaP/GaAs heterojunction bipolar transistor with Schottky contact," *IEEE Electronics Letters*, vol. 35 (8), pp. 670-672, 1999.

[34]. J. N. Burghartz, K. A. Jenkins, D. A. Grutzmacher, T. O. Sedgwick, and C. L. Stanis, "High performance emitter-up/down SiGe HBTs," *IEEE Electron Device Letters*, vol. 15 (9), pp. 360-362, 1994.

[35]. A. Gruhle, H. Kibbel, C. Mahner, and W. Mroczek, "Collector-up SiGe heterojunction bipolar transistors," *IEEE Trans. on Electron Devices*, vol. 46 (7), pp. 1510-1513, 1999.

[36]. J.-S. Rieh, J. Cai, T. Ning, A. Stricker, and G. Freeman, "Reverse active mode current characteristics of SiGe HBTs," *IEEE Trans. On Electron Devices*, vol. 52(6), pp. 1219-1222, 2005.

[37]. W-M. L. Kuo, A. Appaswamy, R.Krithivasan, M. Bellini, J.D. Cressler, and G. Freeman," Reverse active operation of 200 GHz SiGe HBTs," in *Proceedings of ISDRS*, 2005, pp. 183-184.

[38]. ISE TCAD, Version 10, DESSIS Manual.

[39]. G. Wang, H-C. Yuan, Z. Ma," Ultrahigh-performance 8 GHz SiGe power HBT," *IEEE Electron Device Letters*, vol. 27(5), pp. 371-373, 2006.

[40]. J. J. H. van den Biesen, "A simple regional analysis of transit times in bipolar transistors," *Solid State Electronics*, vol. 29, pp. 529-534, 1986.

[41]. C.T. Chuang, K. Chin, J.M.C. Stork, G.L. Patton, E.F. Crabbè, and J.H. Confort, "On the Leverage of High-f_T Transistors for Advanced High-speed Bipolar Circuits" *IEEE Journal of Solid-State Circuits*, vol. 27, no. 2, pp 225-228, Feb. 1992.

[42]. A. P. Gnana Prakash, A. K. Sutton, R. M. Diestelhorst, G. Espinel, J. Andrews, B. Jun, J. D. Cressler, P. W. Marshall, and C. J. Marshall, "The effects of irradiation temperature on the proton response of SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3175-3181, Dec. 2006.

[43]. A. K. Sutton, B. M. Haugerud, A. P. Gnana Prakash, G. Espinel, B. Jun, J. D. Cressler, P. W. Marshall, C. J. Marshall, R. Ladbury, F. Guarin and A. J. Joseph, "A comparison of Gamma and proton radiation effects in 200 GHz SiGe HBTs," *IEEE Transactions on Nuclear Science*, vol. 52, no. 6, pp. 2358-2365, Dec. 2005.

[44]. L.J. Choi, A. Shibaja-Hernandez, S.V. Huylenbroeck, and S. Decoutere, "SiGe HBTs with normal high-speed emitter-up and reverse low-power collector-up operation" *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 358-364, May 2008.

[45]. A. Appaswamy, B. Jun," The effects of proton irradiation on 90nm strained silicon CMOS on SOI devices," *Proceedings of the Radiation Effects Data Workshop*, pp. 62-65, 2006.

[46]. A. Appaswamy, M. Bellini," Impact of scaling on inverse-mode operation of SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1492-1501, 2007.

[47]. A. Appaswamy, S. Phillips, J. D. Cressler," Optimizing inverse mode SiGe HBTs to heavy-ion-induced single event upset," *IEEE Electron Device Letters*, vol. 30, no. 5, pp 511-513, 2009.

[48]. A. Appaswamy, J. D. Cressler," A novel base current phenomenon in SiGe HBTs operating in inverse mode," *Proceedings of ESSDERC.*, pp. 350-353, 2007.

[49]. P. G. Drennan," Device mismatch in BiCMOS technologies," *Proceedings of BCTM*, pp. 104-111, 2002.

[50]. R. Difrenza, J. C. Vildeuil, P. Llinares, and G. Ghibaudo," Impact of grain number fluctuations in the MOS transistor gate on matching performance," *Proceedings of ICTM*, pp. 244-249, 2003.

[51]. J. B. Johnson, T. B. Hook, and Y-M. Li," Analysis and modeling of threshold voltage mismatch for CMOS at 65nm and beyond," *IEEE Electron Device Letters*, vol. 29, no. 7, pp 802-804, 2008.

[52]. P. Andricciola, and H. P. Tuinhout," The temperature dependence of mismatch in deep-submicrometer bulk MOSFETs," *IEEE Electron Device Letters*, vol. 30, no. 6, pp. 690-692, 2009.

[53]. S. Mennillo, A. Spessot, L. Vendarme, and L. Bortesi," An analysis of temperature impact on MOSFET mismatch," *Proceedings of ICMTS*, pp. 56-61, 2009.

[54]. A. Siligaris, G. Pailloncy, S. Delcourt, R. Valentin, S. Lepilliet, F. Daneville, D. Gloria, and G. Dambrine," High frequency and noise performances of 65-nm MOSFET at liquid nitrogen temperature," *IEEE Transactions on Electron Devices*, vol. 53, no. 8, pp. 1902-1908, 2006.

[55]. W. Zhao, Y. Cao, F. Liu, K. Agarwal, D. Acharya, S. Nassif, and K. Nowka," Rigorous extraction of process variations for 65 nm CMOS design," *Proceedings of ESSDERC*, pp. 89-92, 2007.

[56]. N. Wils, H. P. Tuinhout, and M. Meijer," Characterization of STI edge effects on CMOS variability," *IEEE Transactions on Semiconductor Manufacturing*, vol. 22, no. 1, pp. 59-65, 2009.

[57]. P. Fang, K. K. Hung, P. K. Ko, and C. Hu," Hot-electron induced traps studied through the random telegraph noise," *IEEE Electron Device Letters*, vol. 12, no. 6, pp. 273-275, 1991.

[58]. T. K. Thrivikraman, A. Appaswamy, S. D. Phillips, A. K. Sutton, E. P. Wilcox, and J. D. Cressler," A novel device structure using a shared-subcollector, cascoded inverse mode SiGe HBT for enhanced radiation tolerance," *accepted for publication at BCTM*, 2009.

[59]. A. Appaswamy, P. Chakraborty, and J. D. Cressler," Cryogenic matching performance of 90nm MOSFETs," *under review for publication in ISDRS*, 2009.